



IBM Microelectronics

# Automated Large Block Placement Strategies

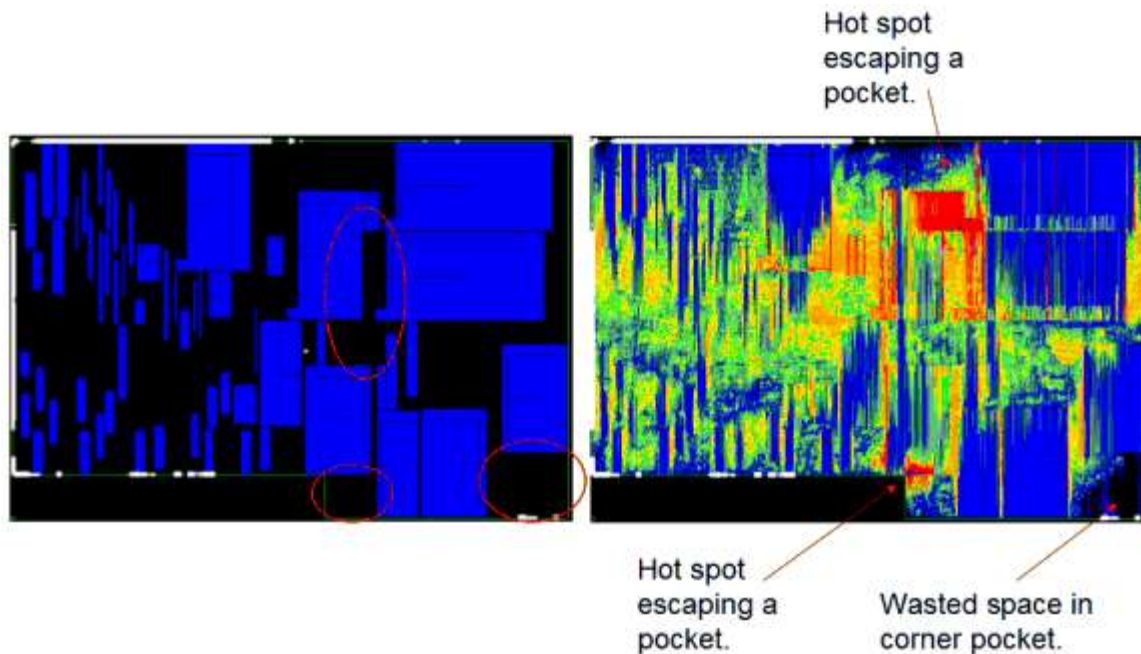
Greg Ford  
IBM Microelectronics

# Introduction

- One of the most fundamental processes in physical design is large block placement – but the best method for this is still generally manual placement.
- What are some of the currently utilized strategies for Automated Large Block Placement?
  - What are the limitations that hinder wider adoption of these methods?
- What are further strategies that can be used to overcome these limitations?

# Extension of Small-Cell Algorithms

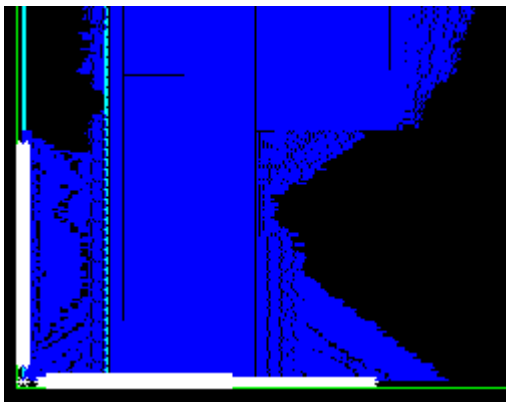
- One class of strategies involves extending the use of algorithms that place small cells in the design.
  - The first issue with this is modeling of blockage associated with placement of large cells, which is not an issue with “dust logic”.



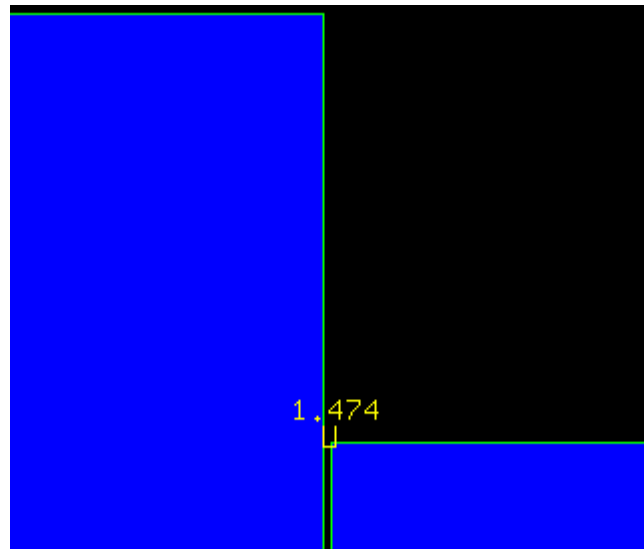
# Extension of Small-Cell Algorithms (cont.)

- These types of algorithms also generally have limited modeling of design requirements associated with large blocks.

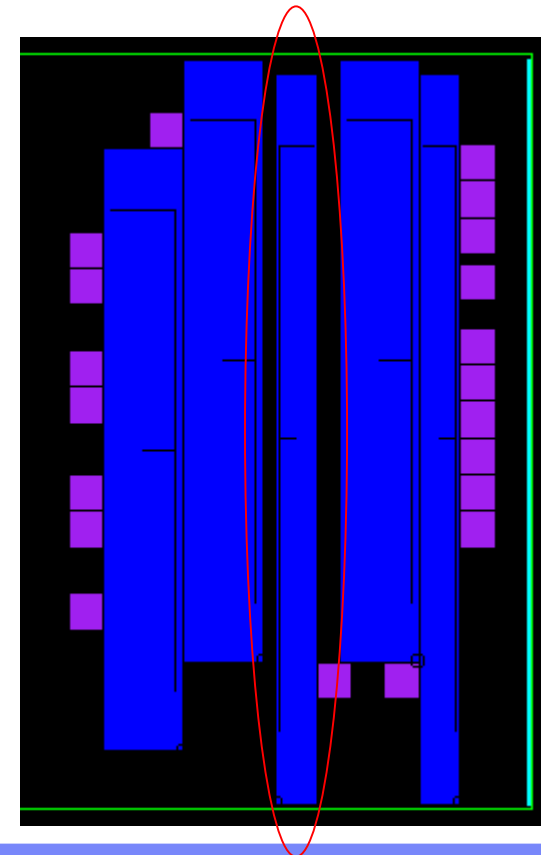
Affinity Logic



Spacing/Abutment

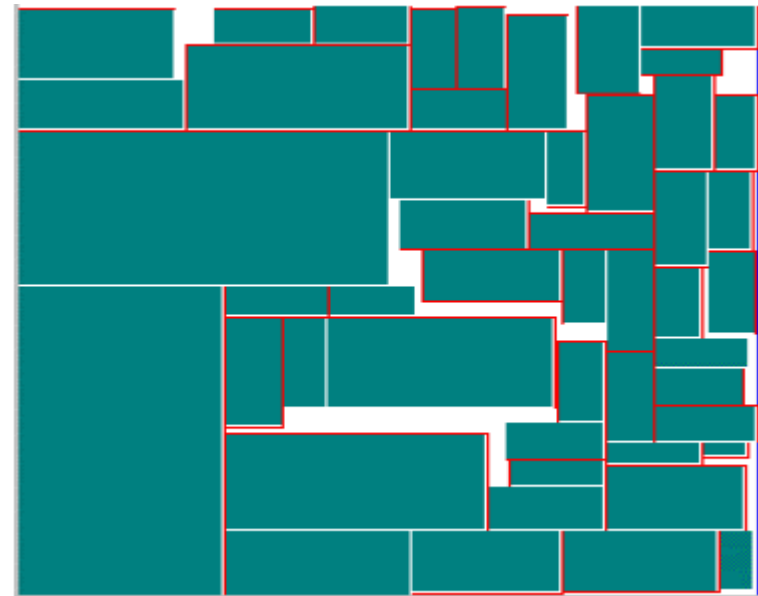
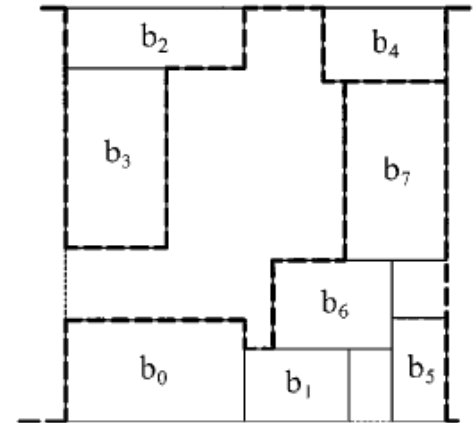


Decap Placement



# Packing Algorithms

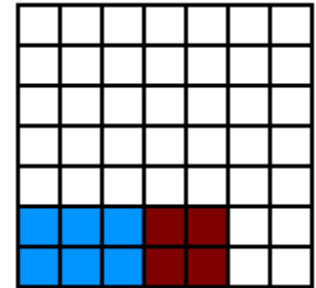
- Another class of strategies is to employ packing techniques to organize large blocks wrt design edges & each other.
- These methods still suffer from tendencies to create “pocketing” and limited modeling of large block design requirements.



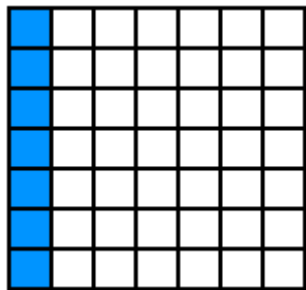
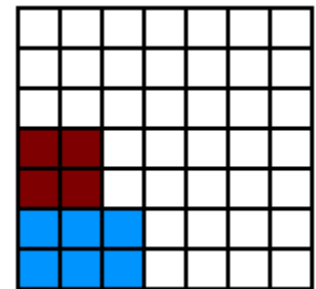
# Enforcing Design Rules by Grouping

- Organize large blocks into groups / subgroups hierarchically.
- Evaluate group placements within a block-level grid.
- This allows for easy use of abutment and aligned groupings, which in turn enforces design rules.

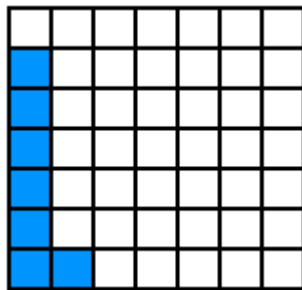
Horizontal Subgroup



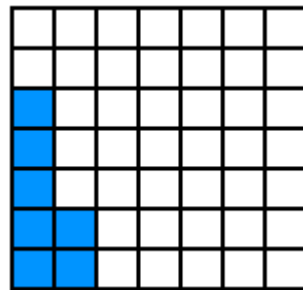
Vertical Subgroup



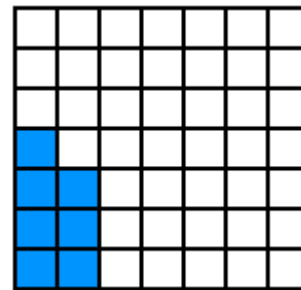
OK



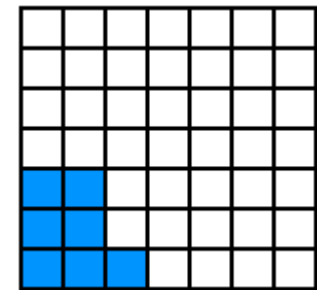
NO



NO



OK

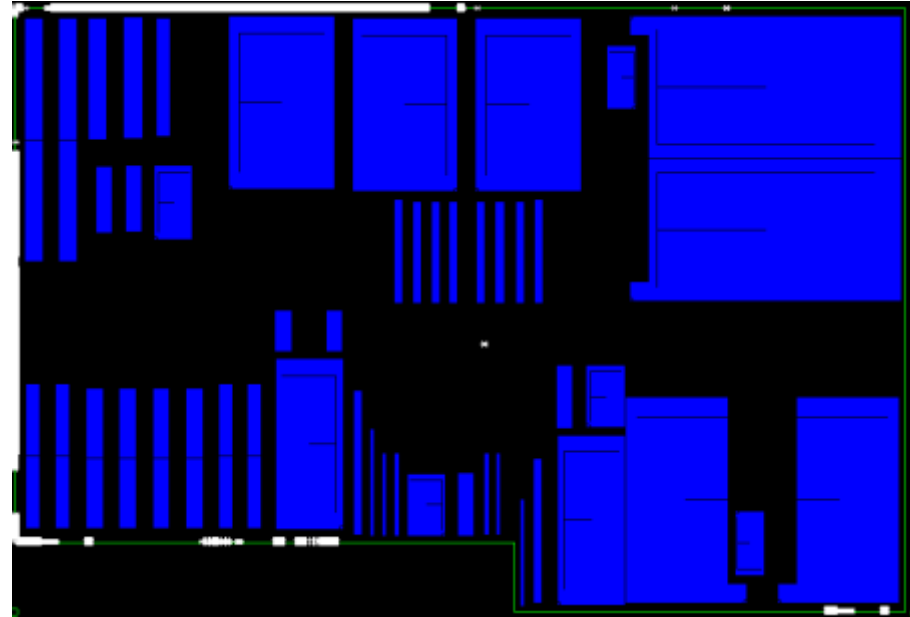
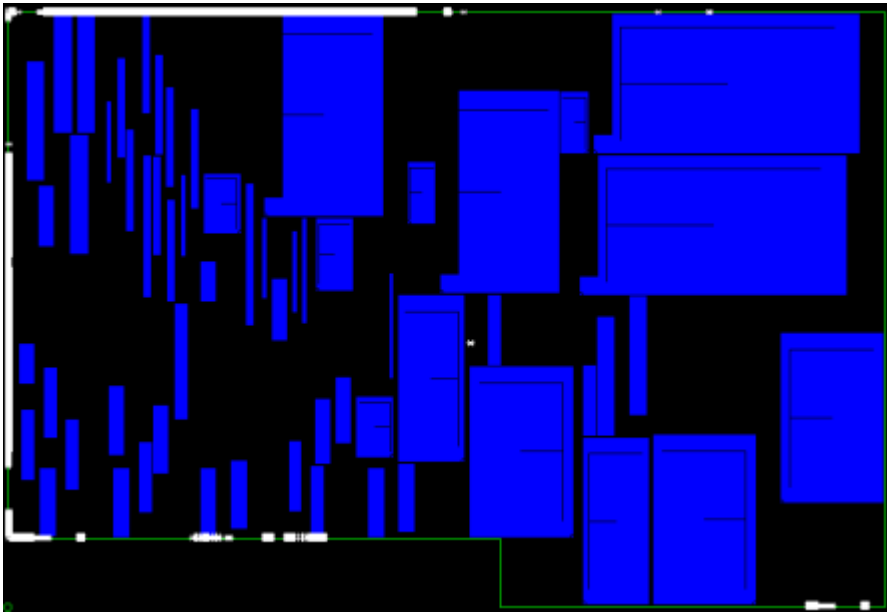


NO

# Creating Placement Regularity

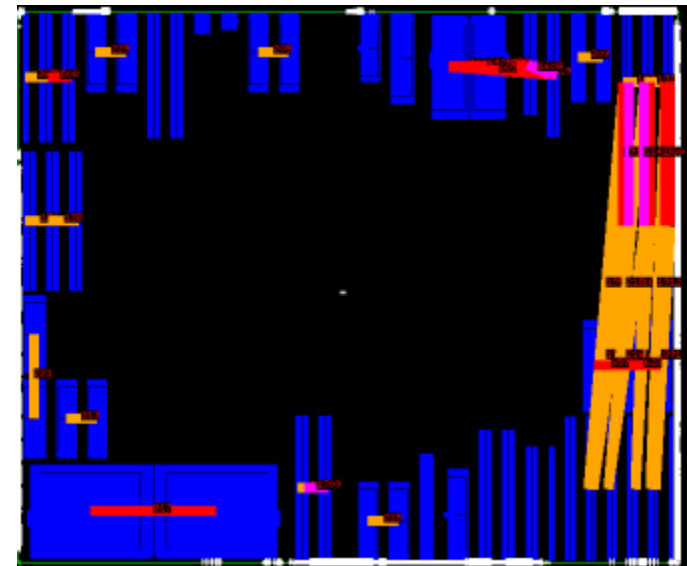
- Humans have a natural desire for order, and manually created placements reflect that.
  - This orderly placement generally leads to better QoR (wiring congestion / timing slacks), further driving acceptance.

Which of these floorplans would you rather have?



# Creating Placement Regularity (cont.)

- Organizing large blocks into groupings gets us part of the way towards regularity. Memories will be banked together, similar to a manual placement.
- To create inter-group regularity, associations between groups and with design edges need to be introduced.
  - Leverage packing algorithms to create alignment between groups and design edges.
  - Leverage associations between groups to promote reasonable inter-group alignment.





# Conclusion

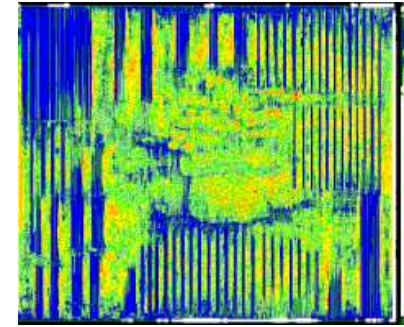
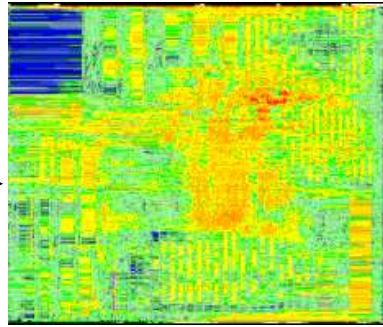
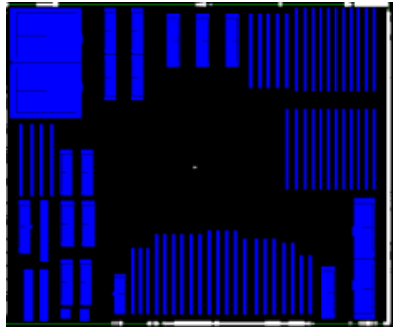
- Large block placement is generally a manual process because current methods do not produce results that designers find desirable.
  - Increasing design sizes add pressure for automated solutions.
- Current methods show limited flexibility with design rules, are prone to leaving suboptimal congestion situations and generate complex layouts that are hard for designers to debug.
- By using block groupings and leveraging placement packing and inter group associations, we can generate correct by construction placements that are understandable to designers, have reasonable QoR and minimize TAT.

# Backup

# Example 1: High Congestion Design

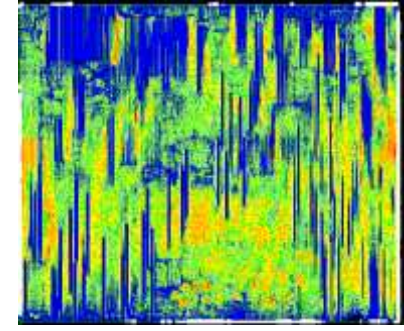
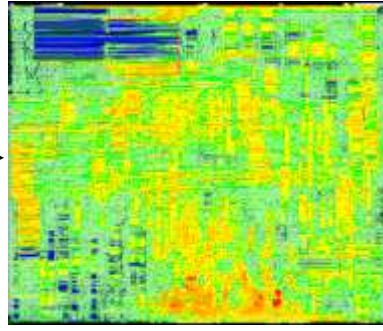
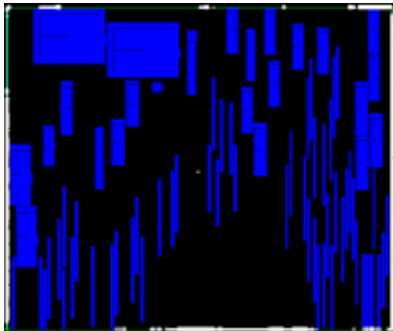
Wire Cng  
Tmg Slack  
(TAT)

Manual



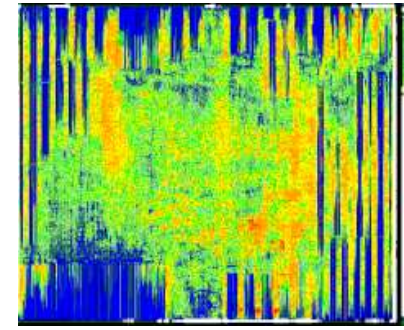
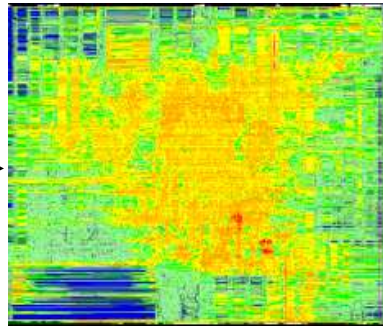
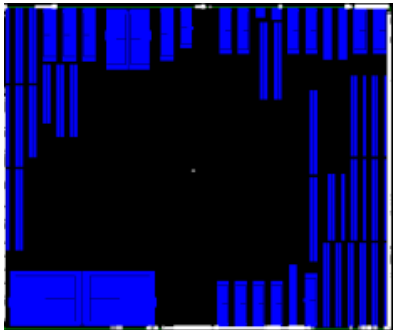
81.2%  
100ps  
(weeks)

Current  
Method



81.3%  
100ps  
(116m)

New  
Method



81.9%  
88ps  
(21m)

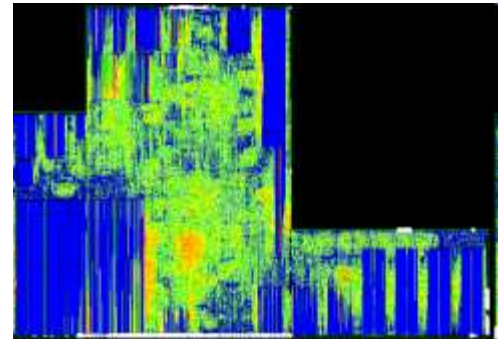
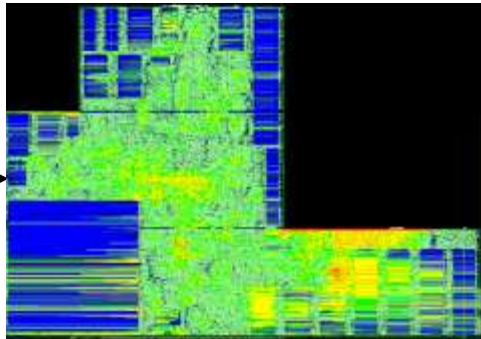
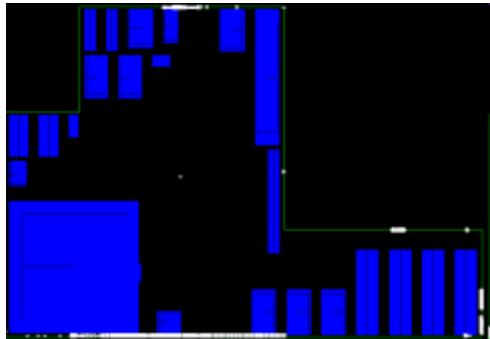
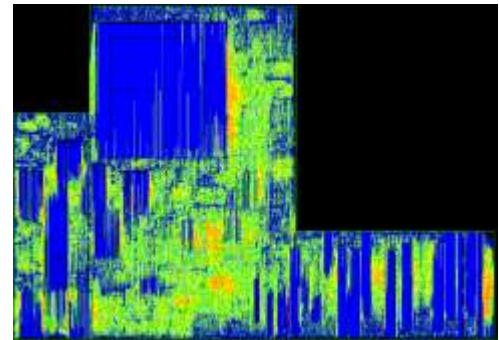
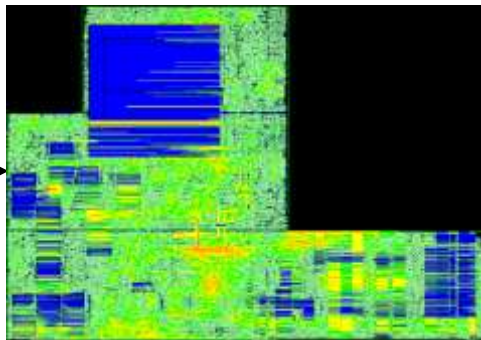
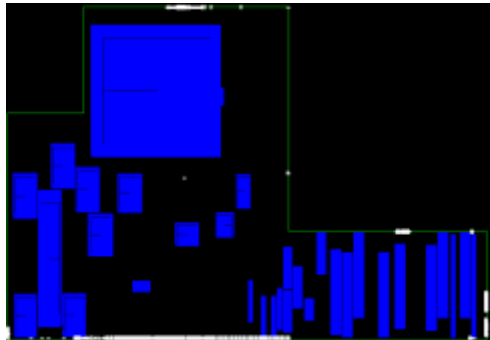
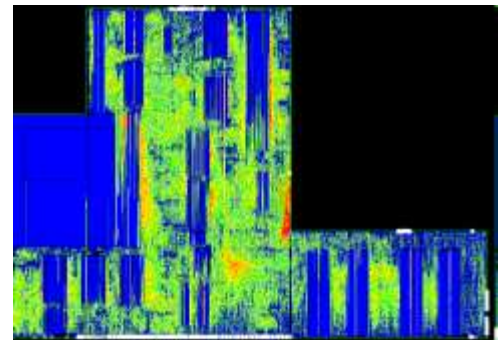
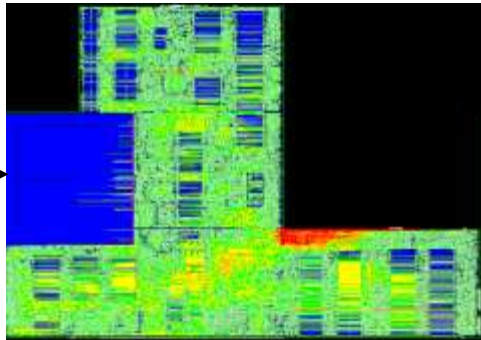
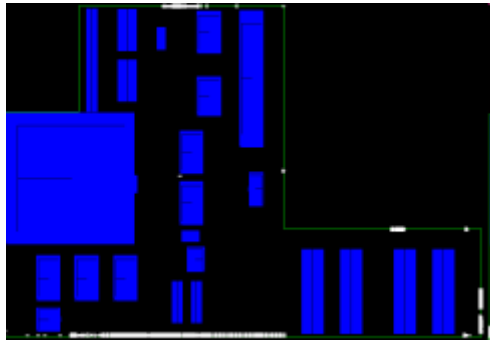
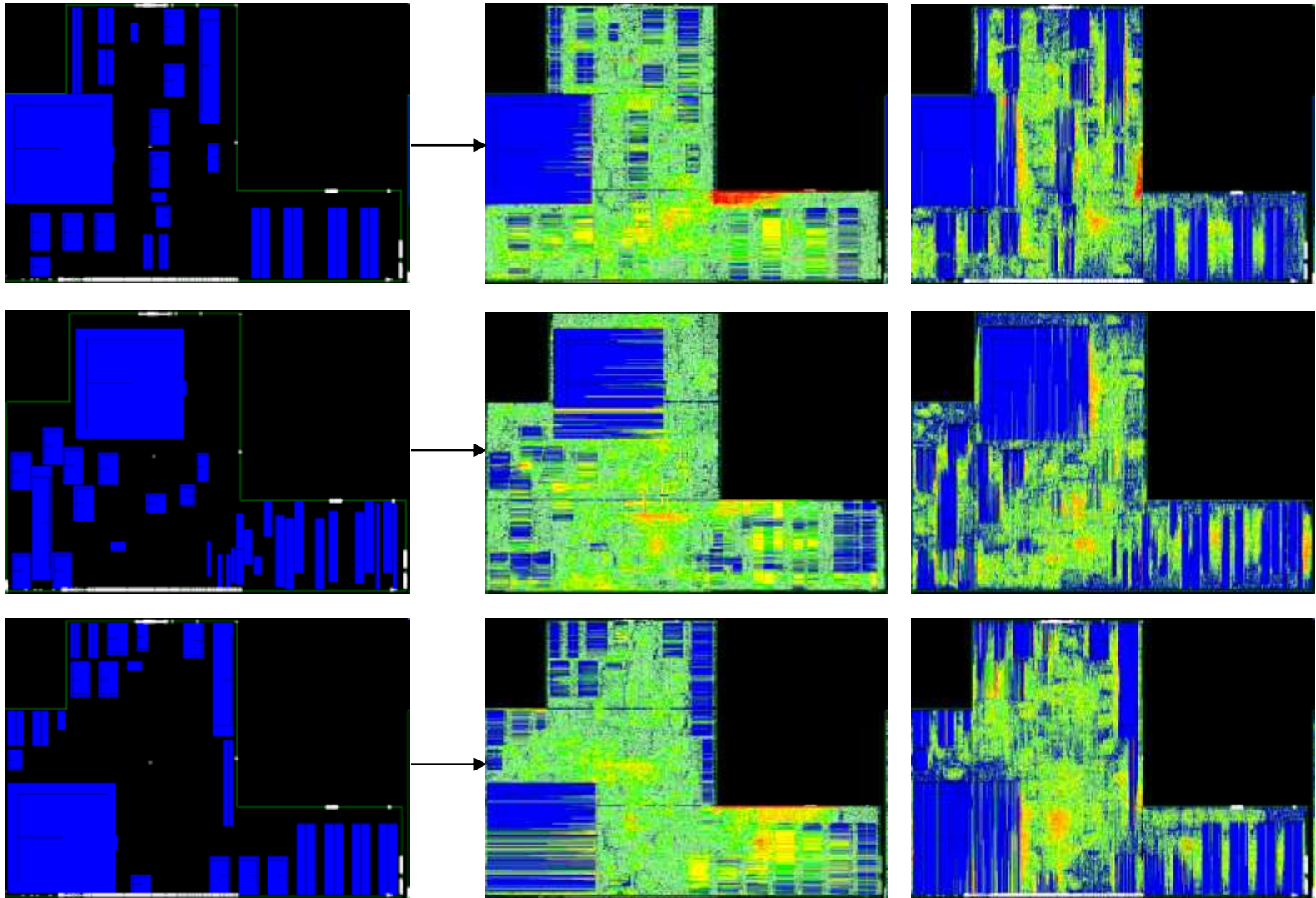
# Example 2: Small Rectilinear Design

Wire Cng  
Tmg Slack  
(TAT)

81.4%  
100ps  
(weeks)

80.7%  
100ps  
(50m)

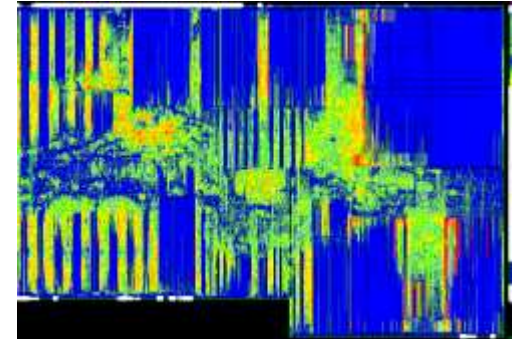
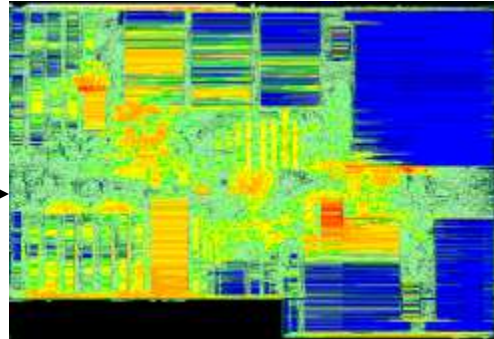
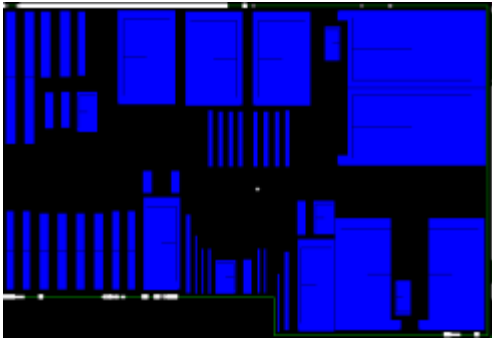
81.1%  
100ps  
(2m)



# Example 3: Large Rectilinear Design

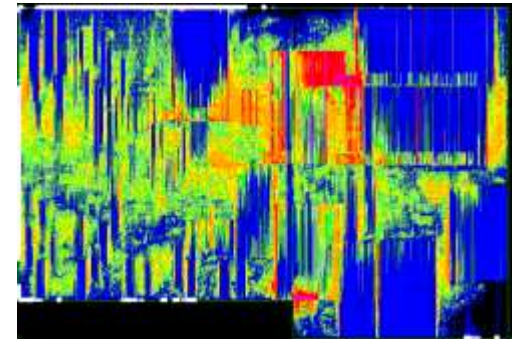
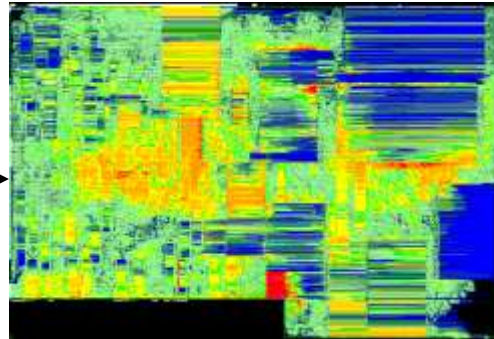
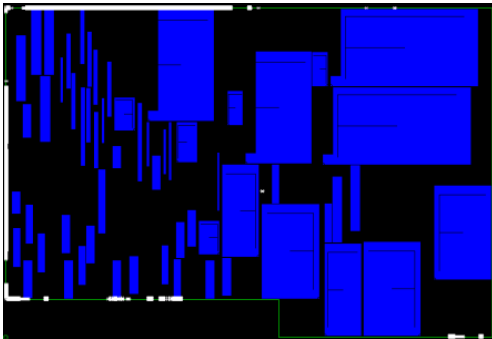
Wire Cng  
Tmg Slack  
(TAT)

Manual



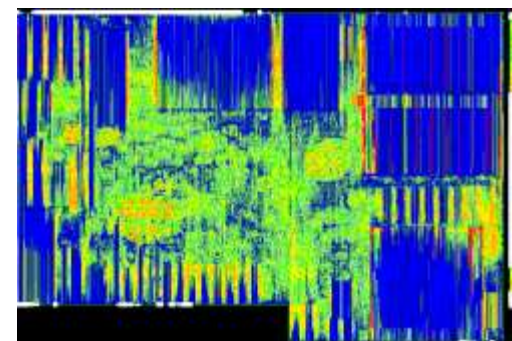
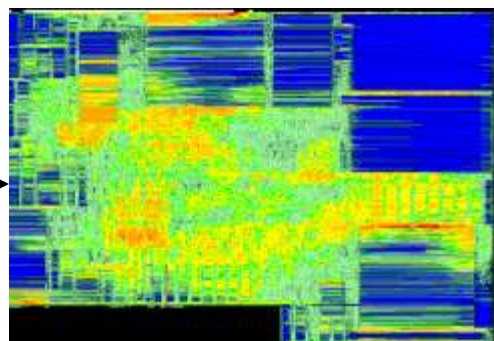
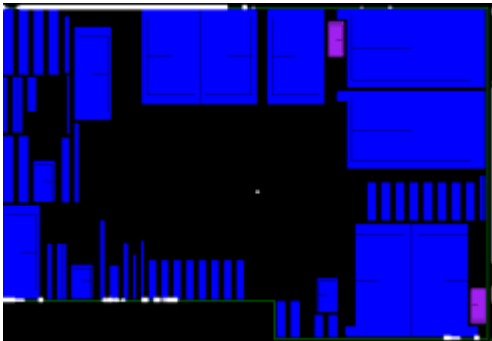
81.0%  
-304ps  
(weeks)

Current  
Method



82.8%  
-500ps  
(67m)

New  
Method



80.9%  
-180ps  
(6m)