Synthesis of Low Power Clock Trees for Handling Power-supply Variations

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Outline

• Clock distribution networks and challenges
• Problem definition
• Parameters affecting clock skew in clock trees
  • Analyze the parameters, variations and their effect on clock skew.
  • Propose techniques to reduce the clock skew.
• Our approach
• Experimental setup and Results
• Conclusions
Clock distribution networks

- **Challenges of clock network synthesis**
  - Satisfy clock skew constraints in the presence of variations.
  - Reduce the power dissipated. (Metric: Capacitance.)

- **Popular structures**
  - Clock trees - Relatively low variation-tolerance, Low capacitance.
  - Clock meshes - High variation-tolerance, High capacitance.
  - Hybrid (mesh + tree, tree + cross-links)

- **Focus of our work: Clock tree structures**
  - Analyze the parameters and variations affecting clock skew.
  - Propose techniques to reduce the clock skew.
Problem definition

Terminology

• Local sink pairs
  • Sink pairs closer than a specified distance ($L$).
    $L$ : Local skew distance.

• Local clock skew (LCS)
  • Clock skew between any local sink pair.

• Maximum local clock skew (MLCS)
  • Many such local sink pairs.
  • Maximum LCS among them.
Problem definition
Based on ISPD 2010 contest problem

- **Given**
  - Clock source, sink and blockage locations.
  - Local skew distance, $L$.
  - MLCS limit.
  - Slew limit.
  - Inverter and wire library.
  - Power-supply and wire-width variations (Uniform distribution).

- **Construct a low capacitance (power) clock tree**
  - **Satisfy slew constraint:** Signal slew < Slew limit.
  - **Satisfy blockage constraint:** Inverters cannot be placed over blockages.
  - **Satisfy MLCS constraint:** $95^{\text{th}}$ percentile of MLCS, $MLCS_{95\%} < \text{MLCS limit}$. 
Parameters affecting clock skew

- **Clock skew parameters**
  - Number of sinks, $N$.
  - Number of buffer levels, $B$.
  - Delay variation per buffer stage, $\sigma_0$.
    - Buffer stage = Buffer + Interconnect it drives.
    - $\sigma_0$ is the standard deviation of delay per buffer stage.
Parameters affecting clock skew

Clock skew under variations

- **Clock tree** $T_D$
  - Identical path delays from source to sinks.
    - Normal distribution with same mean and variance.
  - Possible overlapping paths.
  - Clock skew is $R_D$.

- **Clock tree** $T_I$ *(Hypothetical)*
  - Similar to $T_D$.
  - Assume: No overlapping paths.
  - Clock skew is $R_I$.

- $P(R_D < z) \geq P(R_I < z)$
  - $E(R_I) \geq E(R_D)$ (from [4] and [5])

- $P(R_D < z) \geq P(R_I < z)$
  - $R_{I, 95\%} \geq R_{D, 95\%}$

\[
R_{D, 95\%} = \alpha \cdot R_{I, 95\%} \quad (where \ 0 \leq \alpha \leq 1)
\]

Parameters affecting clock skew

Clock skew under variations

- \( R_{D, 95\%} = \alpha \cdot R_{I, 95\%} \) (where \( 0 \leq \alpha \leq 1 \))
  - Asymptotic formulae for \( E(R_i) \) and \( Var(R_i) \).
  - For given \( N, B \) and \( \sigma_0 \).
  - Sample set large => Assume normal distribution for \( R_i \).
  \[ R_{I, 95\%} \sim E(R_i) + 2 \cdot \sqrt{Var(R_i)} \]

- \( R_{D, 95\%} \sim \alpha \cdot [ E(R_i) + 2 \cdot \sqrt{Var(R_i)} ] \)

- **Formula for 95\textsuperscript{th} percentile of clock skew (R) for general clock tree.**
  - Include nominal clock skew (NCS).
  \[ R_{95\%} \sim NCS + \alpha \cdot [ E(R_i) + 2 \cdot \sqrt{Var(R_i)} ] \]
  - Empirically estimate \( \alpha \).
Parameters affecting MLCS

• **Wire-width variations (vs) Power-supply variations**
  - Low slew => Small DC-connected subtrees.
  - Effect of wire variations relatively small compared to power-supply variations.

• **Our focus: Power-supply variations**
  - Delay variation per buffer stage, $\sigma_0$:
    - $\sigma_0$ of buffer stage $\sim \sigma_0$ of buffer.
Parameters affecting MLCS

- **LCS parameters**
  - **Number of buffer levels, \( B \):**
    - Subtree of the NCA (nearest common ancestor) of local sink pair.
  - **Number of sinks, \( N \):**
    - Subtree of the NCA of local sink pair.
    - Number of level 1 buffers (bottom-up from sinks).

- **MLCS parameters**
  - \( \sigma_0 \), \( N \) and \( B \) values that give the highest 95% LCS among all local sink pairs.
Parameters affecting MLCS

Power-supply variations

- **ISPD 2010 contest**
  - Inverter modeled as a single point.
  - Many inverters can be placed at a single location.
    - Parallel inverters to increase the drive strength.
    - Buffers.

- **Types of Monte-Carlo (MC) simulations**
  - **ISPD MC simulations.** (ISPD problem.)
    - Inverters placed at same location could get different voltages.
    - Same as the contest simulations.
  - **SLSV MC simulations.** (SLSV problem.)
    - Inverters placed at same location get identical voltages.
    - SLSV : Single Location Single Voltage.
Observations on $\sigma_0$
Key Technique - ISPD problem

- **Use parallel inverters to reduce $\sigma_0$:**
  
  Note: Short circuit power dissipation could increase.
  - Not captured if only capacitance is used as metric for power dissipation.

![Graph 1: Probability vs. Delay for 1 inverter](image1)

![Graph 2: Probability vs. Delay for 30 parallel inverters](image2)
Observations on $\sigma_0$

Key Techniques - SLSV problem

- Buffers (chain of 2 inverters) have lower $\sigma_0$ than inverters.
  - Inverters of a buffer (chain of 2 inverters) get identical power-supply voltages.
  - Use buffers (chain of 2 inverters).

- Lower buffer input slew => Lower $\sigma_0$.
  - Try to maintain low slew in the clock tree.

- No significant change in $\sigma_0$ for different buffer sizes.
  - At low input slews.
  - For loads at which buffers are inserted to avoid slew constraint violations.

In our work: A single buffer size is used in entire clock tree (for simplicity).
Observations on $N$ and $B$

Key Techniques

• However, buffer size determines $N$ and $B$.
  • ISPD and SLSV problem.

• Lower values of $N$ and $B$ $\Rightarrow$ Lower $MLCS_{95\%}$.
  • Difficult to estimate the buffer size that gives lower $N$ and $B$.
    - Non-uniform sink distribution.
    - Blockages.
    - Drive strength (vs) Upstream capacitance presented.

• We perform a linear search to find the desired buffer size.
Our approach

Given a buffer size

- Construct low nominal skew clock tree
  - Deferred Merge Embedding (DME) algorithm
    - Merging strategy
    - Buffer insertion strategy
      - Avoid slew and blockage constraint violations
    - Buffer modeling

- Use the formula for $R_{95\%}$ to estimate $MLCS_{95\%}$
Our approach
Buffer modeling

  - Iterative approach to model buffer.

- Use NGSPICE for buffer modeling.
  - Stringent MLCS constraints.

Our approach

Two stages

Stage 1: Perform a linear search for the desired buffer size

Given a buffer size

- Construct low nominal skew tree (DME algorithm)
  - Merging
  - Buffer insertion strategy
    - Avoid slew and blockage constraint violations
- Buffer modeling (Use fast buffer modeling)
- Use the formula for $R_{95\%}$ to estimate $MLCS_{95\%}$

Stage 2: Construct low nominal skew tree

(use buffer size determined from stage 1)

- Similar to above EXCEPT
  - Buffer modeling (use NGSPICE)
  - Fine tune nominal clock skew (use NGSPICE)

Reason:
Using NGSPICE while searching for desired buffer size - Expensive!
Experimental setup

• **Benchmark circuits**
  - ISPD 2010 contest benchmark circuits [7].
  - More than 1000 sinks. (MLCS constraint of 7.5ps or less.)
  - Based on Intel and IBM microprocessor designs (scaled to 45nm).

• **Variations**
  - Power-supply variations: ±7.5%.
  - Wire-width variations: ± 5%.

• **Power-supply variation (±7.5%)**
  - Only $V_{dd}$.
    - We present the results for these simulations.
  - Share between $V_{dd}$ and $V_{ss}$.
    - Similar or lower $MLCS_{95\%}$.

## Results

Using parallel inverters to solve ISPD problem

<table>
<thead>
<tr>
<th>BM</th>
<th>MLCS limit (ps)</th>
<th>nom</th>
<th>ISPD MC</th>
<th>SLSV MC</th>
<th>Cap (fF)</th>
<th>Runtime (secs)</th>
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Results
Using buffers (2 layers of parallel inverters) to solve SLSV problem

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## Results

Using parallel inverters to solve ISPD problem
500 MC simulations

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## Results

Using buffers (2 layers of parallel inverters) to solve SLSV problem
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Results
Comparison of ISPD MC using inverters

  - Tree structure.
  - Best results among the top three teams.

- On an average: Cap of our work = 1.00, Cap of [1] = 1.22x.
Results

Comparison of ISPD MC using inverters

  - Tree + cross-links structure.
  - Use inverters.

- On an average: Cap of our work = 1.00, Cap of [3] = 0.79x.
Results
Comparison of ISPD MC using buffers

  - Tree + cross-links structure.
  - Use buffers.
- On an average: Cap of our work = 1.00, Cap of [3] = 0.83x.
Results
Comparison of SLSV MC using buffers

  - Mixed tree-mesh structure.
  - Note: They use single buffer at any location.

- On an average: Cap of our work = 1.00, Cap of [2] = 2.33x.
Conclusions

• **Our contributions**
  - Identified, analyzed parameters that have high impact on MLCS.
  - Quick estimate of MLCS using these parameters.
    - Avoid expensive MC simulations.
  - Simple two-stage technique to meet MLCS constraints.

• **Clock tree structure**
  - Can handle stringent MLCS constraints for most of the contest benchmarks.
  - Analysis of the variations
    - Helps to check if clock tree structures satisfy skew constraints.
Thank you