2017 International Symposium on Physical Design

With a Tribute to Prof. Satoshi Goto

Portland-Lake Oswego, Oregon, March 19-22, 2017

http://www.ispd.cc

Proceedings: http://dl.acm.org/citation.cfm?id=3036669

PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI, biological or other advanced technology systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance optimization and design for manufacturing.

Regular presentations are 30 minutes.

SUNDAY, March 19

5:30 – 7:00pm: Evening Reception

MONDAY, March 20

7:15 – 8:15am: Breakfast

8:15 – 9:30am: Welcome & Monday Morning Keynote

Host: Mustafa Ozdal (Bilkent University)

(Keynote) "Technology Options for Beyond CMOS", *Ian Young (Intel)*

9:30 – 10:00am: Morning Break

10:00am – 12:00noon: Session 1: Machine Learning in EDA

Session Chair: David Pan *(The University of Texas at Austin)*

(Invited) "The Quest for The Ultimate Learning Machine", *Pradeep Dubey (Intel)*

(Invited) "Deep Learning in Enhanced Cloud", *Eric Chung (Microsoft)*

"Bilinear Lithography Hotspot Detection", *Hang Zhang, Fengyuan Zhu, Haocheng Li, Evangeline F.Y. Young and Bei Yu*

"Routability Optimization for Industrial Designs at Sub-14nm Process Nodes Using Machine Learning", *Wei-Ting Chan, Pei-Hsin Ho, Andrew B. Kahng and Prashant Saxena*

12:00 – 1:30pm: Lunch

1:30 – 2:30pm: Monday Afternoon Keynote

Host: Prashant Saxena *(Synopsys)*

(Keynote) "Pushing the boundaries of Moore's Law to transition from FPGA to All Programmable Platform", *Ivo Bolsens (Xilinx)*

2:30 – 3:00pm: Session 2: Invited Poster Presentation

(Invited) "How Game Engines Can Inspire EDA Tools Development: A use case for an open-source physical design library", *Tiago Fontana, Renan Netto, Vinicius Livramento, Chrystian Guth, Sheiny Almeida, Laércio Pilla, José Luís Güntzel*

(Invited) "Rsyn – An Extensible Physical Synthesis Framework", *Guilherme Flach, Mateus Fogaça, Jucemar Monteiro, Marcelo Johann and Ricardo Reis*

3:00 – 3:30pm: Poster Session and Afternoon Break

3:30 – 5:30pm: Session 3: Nontraditional Physical Design Challenges

Session Chair: Rickard Ewetz *(University of Central Florida)*

(Invited) "Research Challenges in Security-aware Physical Design", *Ramesh Karri (NYU)*

(Invited) "Challenges and Opportunities: From Near-memory Computing to In-memory Computing", *Soroosh Khoram, Yue Zha, Jialiang Zhang and Jing Li (University of Wisconsin-Madison)*

"Physical Design Considerations of One-level RRAM-based Routing Multiplexers", *Xifan Tang, Edouard Giacomin, Giovanni De Micheli and Pierre-Emmanuel Gaillardon*

"Hierarchical and Analytical Placement Techniques for High-Performance Analog Circuits", *Biying Xu, Shaolan Li, Xiaoqing Xu, Nan Sun and David Z. Pan*

6:00 – 8:00pm: Dinner Banquet

TUESDAY, March 21

7:30 – 8:30am: Breakfast

8:30 – 9:30am: Tuesday Keynote

Host: Kevin Chao (*Intel*)

(Keynote) "Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend", *Lee-Chung Lu (TSMC)*

9:30 – 10:00am: Morning Break

10:00am – 12:00noon: Session 4: Clock and Timing

Session Chair: Gustavo Wilke (*Synopsys*)

(Invited) "Modern Challenges in Constructing Clocks", *Charles J. Alpert (Cadence)*

"Clock Tree Construction based on Arrival Time Constraints", *Rickard Ewetz and Cheng-Kok Koh*

"A Fast Incremental Cycle Ratio Algorithm", *Gang Wu and Chris Chu*

"iTimerM: Compact and Accurate Timing Macro Modeling for Efficient Hierarchical Timing Analysis", *Pei-Yu Lee, Iris Hui-Ru Jiang and Ting-You Yang*

12:00 – 1:30pm: Lunch

1:30 – 3:00pm: Session 5: Routability Consideration

Session Chair: Yue Xu *(Oracle)*

"DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment", *Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, Yibo Lin and David Z. Pan*

"Automatic Cell Layout in the 7nm Era", *Pascal Cremer, Stefan Hougardy, Jan Schneider and Jannik Silvanus*

"Improving Detailed Routability and Pin Access with 3D Monolithic Standard Cells", *Daohang Shi and Azadeh Davoodi*

3:00 – 3:30pm: Afternoon Break

3:30 – 5:30pm: Session 6: Commemoration for Prof. Satoshi Goto

Session Chair: Jinjia Zhou *(Hosei University)*

(Invited) "The Spirit of in-house CAD Achieved by the Legend of Master "Prof. Goto" and his Apprentices", *Yuichi Nakamura (NEC Corp.)*

(Invited) "Generalized Force Directed Relaxation with Optimal Regions and Its Applications to Circuit Placement", *Yao-Wen Chang (National Taiwan University)*

(Invited) "100x Evolution of Video Codec Chips", *Jinjia Zhou (Hosei University)*

(Invited) "Physical Layout after Half a Century: From Back-Board Ordering to Multi-Dimensional Placement and Beyond", *Chung-Kuan Cheng (University of California, San Diego)*

(Invited) "Past, Present and Future of the Research", *Satoshi Goto (Waseda University)*

6:00 – 9:00pm: Dinner party in tribute to Prof. Goto

WEDNESDAY, March 22

7:20 – 8:20am: Breakfast

8:20 – 9:50am: Session 7: Optimization and Placement

Session Chair: Jackey Yan *(Cadence)*

(Invited) "Interesting Problems in Physical Synthesis", *Pei-Hsin Ho (Synopsys)*

"Pin Accessibility-Driven Detailed Placement Refinement", *Yixiao Ding, Chris Chu and Wai-Kei Mak*

"A Fast, Robust Network Flow-based Standard-Cell Legalization Method For Minimizing Maximum Movement", *Nima Karimpour Darav, Ismail S. Bustany, Andrew Kennings and Laleh Behjat*

9:50 – 10:10am: Morning Break

10:10am – 12:20pm: Session 8: FPGA CAD and Contest

Session Chair: Wai-Kei Mak *(National Tsing Hua University)*

(Invited) "CAD Opportunities with Hyper-Pipelining", *Mahesh A. Iyer (Intel)*

"An Effective Timing-Driven Detailed Placement Algorithm for FPGAs", *Shounak Dhar, Mahesh A. Iyer, Saurabh Adya, Love Singhal, Nikolay Rubanov and David Z. Pan*

"Clock-Aware FPGA Placement Contest", *Stephen Yang, Chandra Mulpuri, Sainath Reddy, Meghraj Kalase, Srinivasan Dasasathyan, Mehrdad E. Dehkordi, Marvin Tom and Rajat Aggarwal (Xilinx)*

12:20 – 12:25pm: Closing Remarks

12:25 – 1:30pm: Lunch

1:30 – 6:00pm: Social Event – Multnomah Falls