2020 International Symposium on Physical Design

With a Tribute to Dr. Louis K. Sheffer

Taipei, Taiwan, Sept. 20 – Sept. 23, 2020

www.ispd.cc

PROGRAM

The International Symposium on Physical Design (ISPD) provides a premier forum to exchange ideas and promote research on critical areas related to the physical design of VLSI systems. All aspects of physical design, including its interactions with architecture, behavioral and logic-level synthesis, and back-end performance analysis and verification are within the scope of the symposium. Target domains include semi-custom and full-custom ICs, ASICs, FPGAs, and systems-on-chip/systems-in-package.

Regular presentations are 30 minutes.

SUNDAY, Sept. 20

5:30 – 7:00 pm: Reception

MONDAY, Sept. 21

8:45 – 10:00 am: Welcome and Keynote Address

General Chair Message: Bill Swartz, TimberWolf Systems and University of Texas at Dallas

Keynote Address: "Scalable System and Silicon Architectures to Handle the Workloads of the Post-Moore Era," Ivo Bolsens, Xilinx

10:00 – 10:30 am: Morning Break

10:30 am - 12:30 pm Session 1: Placement
Session Chair: Stephen Yang, Xilinx

"Reinforcement Learning for Placement Optimization," Azalia Mirhoseini, Google Brain (Invited)

"Hill Climbing with Trees: Detail Placement for Large Windows," Mohammad Khasawneh and Patrick Madden

"Via Pillar-aware Detailed Placement," Yong Zhong, Tao-Chun Yu, Kai-Chuan Yang and Shao-Yun Fang

"Soft-Clustering Driven Flip-flop Placement Targeting Clock-induced OCV," Dimitrios Mangiras, Pavlos Mattheakis, Pierre-Olivier Ribet and Giorgos Dimitrakopoulos

12:30 – 2:00 pm: Lunch

2:00 – 3:30 pm Session 2: Breaking New Ground: From Carbon Nanotubes to Packaging
Session Chair: Patrick H. Madden, SUNY Binghamton

"Advances in Carbon Nanotube Technologies: from Transistors to a RISC-V Microprocessor," Gage Hills, MIT (Invited)

"Full-Chip Electro-Thermal Coupling Extraction and Analysis for Wafer-on-Wafer 3D ICs," Sung Kyu Lim, Georgia Tech (Invited)

"Pseudo-3D Approaches for Commercial-Grade RTL-to-GDS Tool Flow Targeting Monolithic 3D ICs," Heechun Park, Bon Woong Ku, Kyungwook Chang, Da Eun Shim and Sung Kyu Lim

3:30 – 4:00 pm: Afternoon Break

4:00 – 5:30 pm Session 3: Machine Learning for Physical Design (1)
Session Chair: Patrick Groeneveld, Cerebras Systems

"Learning from Experience: Applying ML to Analog Circuit Design," Sachin Sapatnekar, University of Minnesota (Invited)

"Transforming Global Routing Report into DRC Violation Map with Convolutional Neural Network," Wei-Tse Hung, Jun-Yang Huang, Yih-Chih Chou, Cheng-Hong Tsai and Mango Chao (Best Paper Award Nominee)

"Lookahead Placement Optimization with Cell Library-based Pin Accessibility Prediction via Active Learning," Tao-Chun Yu, Shao-Yun Fang, Hsien-Shih Chiu, Kai-Shun Hu, Philip Hui-Yuh Tai, Cindy Chin-Fang Shen and Henry Sheng

6:00 – 8:00 pm: Monday Dinner Banquet

TUESDAY, Sept. 22

8:30 – 9:30 am: Tuesday Keynote Address
Session Chair: Mark Po-Hung Lin, National Chiao Tung University

Keynote Address: "Physical Design for 3D Chiplets and System Integration," Cliff Hou, TSMC

9:30 – 10:00 am: Morning Break

10:00 – 11:30 am Session 4:
Circuit Design and Security
Session Chair: David Chinnery, Mentor - A Siemens Business

"Hardware Security for and beyond CMOS Technology," Johann Knechtel, New York University Abu Dhabi (Invited)

"Design Optimization by Fine-grained Interleaving of Local Netlist Transformations in Lagrangian Relaxation," Apostolos Stefanidis, Dimitrios Mangiras, Chrysostomos Nicopoulos, David Chinnery and Giorgos Dimitrakopoulos

"Selective Sensor Placement for Cost-Effective Online Aging Monitoring and Resilience," Hao-Chun Chang, Li-An Huang, Kai-Chiang Wu and Yu-Guang Chen

11:30 – 12:30 pm Session 5: Timing and Clocking
Session Chair: Evangeline Young, Chinese University of Hong Kong

"Synthesis of Clock Networks with a Mode Reconfigurable Topology and No Short Circuit Current," Necati Uysal, Juan Ariel Cabrera and Rickard Ewetz

"Timing Driven Partition for Multi-FPGA Systems with TDM Awareness," Sin-Hong Liou, Sean Liu, Richard Sun and Hung-Ming Chen (Best Paper Award Nominee)

12:30 – 2:00 pm: Lunch

2:00 – 3:30 pm Session 6:
Machine Learning for Physical Design (2)
Session Chair: Ismail Bustany, Xilinx

"Understanding Graphs in EDA: From Shallow to Deep Learning," Bei Yu, Chinese University of Hong Kong (Invited)

"TEMPO: Fast Mask Topography Effect Modeling with Deep Learning," Wei Ye, Mohamed Baker Alawieh, Yuki Watanabe, Shigeki Nojima, Yibo Lin and David Z. Pan (Best Paper Award Nominee)

"DRC Hotspot Prediction at Sub-10nm Process Nodes Using Customized Convolutional Network," Rongjian Liang, Hua Xiang, Diwesh Pandey, Lakshmi Reddy, Shyam Ramji, Gi-Joon Nam and Jiang Hu

3:30 – 4:00 pm: Afternoon Break

4:00 – 5:30 pm Session 7:
Commemoration for Dr. Louis K. Scheffer
Session Chair: Marilyn Wolf, University of Nebraska-Lincoln

Presentations outlining the work and achievements of Dr. Louis K. Scheffer
"A Lifetime of CAD, and a Cloudy Crystal Ball", Louis K. Scheffer

6:00 – 9:00 pm: Tuesday Dinner Banquet

WEDNESDAY, Sept. 23

8:45 – 9:45 am: Wednesday Keynote Address
Session Chair: Iris Hui-Ru Jiang, National Taiwan University (NTU)

Keynote Address: "Physical Verification at Advanced Technology Nodes and the Road Ahead," Juan Rey, Mentor - A Siemens Business

9:45 – 10:15 am: Morning Break

10:15 am – 11:45 pm Session 8:
ISPD 2020 Contest Results and Poster Presentations
Session Chair: Marvin Tom, Cerebras Systems

"ISPD 2020 Wafer-Scale Deep Learning Accelerator Placement Contest: Overview and Results," Marvin Tom, Cerebras Systems

Short video presentations by top 5 winning teams

Awards Ceremony

11:45 am – 12:00 pm: Closing Remarks

12:00 – 12:30 pm: Boxed Lunch

12:30 – 6:00 pm: Social Activity – TSMC Museum