2018 International Symposium on Physical Design

With a Tribute to Professor Te Chiang Hu

Monterey, California, March 25 - 28, 2018

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PRELIMINARY PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI, biological or other advanced technology systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance optimization and design for manufacturing.

Regular presentations are 30 minutes.

SUNDAY, March 25

5:30 – 7:00 pm: Reception

MONDAY, March 26

8:45 – 10:00 am: Welcome and Keynote Address

General Chair Message: Chris Chu (Iowa State Univ.)

Keynote: "Challenges and Opportunities in Automotive, Industrial, and IoT Physical Design," Anthony Hill (Texas Instruments Inc., invited)

10:00 – 10:30 am: Morning Break

10:30 am - 12:00 pm Session 1: Finding the Golden Tree in the Forest!

Session Chair: Gary Yeap (Synopsys Inc.)

"Wot the L: Analysis of Real versus Random Placed Nets, and Implications for Steiner Tree Heuristics," Andrew B. Kahng, Christopher Moyes, Sriram Venkatesh, and Lutong Wang

"Prim-Dijkstra Revisited: Achieving Superior Timing-driven Routing Trees," Charles J. Alpert, Wing-Kai Chow, Kwangsoo Han, Andrew B. Kahng, Zhuo Li, Derong Liu, and Sriram Venkatesh (Best Paper Award Nominee)

"Construction of All Rectilinear Steiner Minimum Tree on the Hanan Grid," Sheng-En David Lin and Dae Hyun Kim

12:00 – 1:30 pm: Lunch

1:30 – 3:30 pm Session 2: FPGA Special Session

Session Chair: Sabya Das (Xilinx Inc.)

"Challenges in Large FPGA based Logic Emulation Systems," William N. Hung and Richard Sun (Synopsys Inc., invited)

"Flexibility: FPGAs and CAD in Deep Learning Accelerations," Gordon Chiu (Intel Corp., invited)

"Exploration and Tradeoffs of different Kernels in FPGA Deep Learning Applications," Elliott Delaye and Ashish Sirasao (Xilinx Inc., invited)

"Architecture Exploration of Standard-Cell and FPGA-Overlay CGRAs Using the Open-Source CGRA-ME Framework," Xander Chin, Steven Niu, and Jason Anderson (University of Toronto, invited)

3:30 – 4:00 pm: Afternoon Break

4:00 – 5:30 pm Session 3: Design Flow and Power Grid Optimization

Session Chair: Mahesh Iyer (Intel Corp.)

"Concurrent High Performance Processor Design: From Logic to PD in Parallel," Leon Stok (IBM Corp., invited)

"Towards a VLSI Design Flow Based on Logic Computation and Signal Distribution," Andre Inacio Reis (Universidade Federal do Rio Grande do Sul, invited)

"Power Grid Reduction by Sparse Convex Optimization," Wei Ye, Meng Li, Kai Zhong, Bei Yu, and David Z. Pan

6:00 – 8:00 pm: Dinner Banquet

TUESDAY, March 27

9:00 – 10:00 am: Tuesday Keynote Address

Keynote: "Silicon Compilers - Version 2.0," Andreas Olofsson (DARPA)

10:00 – 10:30 am: Morning Break

10:30 am – 12:30 pm Session 4: Statistical and Machine Learning-Based CAD

Session Chair: (TBD)

"Machine Learning Applications in Physical Design: Recent Results and Directions," Andrew Kahng (UC San Diego, invited)

"Machine Learning for Feature-Based Analytics," Li-C. Wang (UC Santa Barbara, invited)

"Data Efficient Lithography Modeling with Residual Neural Networks and Transfer Learning," Yibo Lin, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Meng Li, and David Z. Pan

12:30 – 2:00 pm: Lunch

2:00 – 3:30 pm Session 5: Three Shades of Placement!

Session Chair: Joseph Shinnerl (Mentor, a Siemens Business**)**

"Compact-2D: A Physical Design Methodology to Build Commercial-Quality Face-to-Face-Bonded 3D ICs," Bon Woong Ku, Kyungwook Chang, and Sung Kyu Lim (Best Paper Award Nominee)

"Analog Placement Constraint Exploration with the Application to Layout Retargeting," Biying Xu, Bulent Basaran, Ming Su, and David Z. Pan

"Pin Assignment Optimization for Multi-2.5D FPGA-based Systems," Wan-Sin Kuo, Shi-Han Zhang, Wai-Kei Mak, Richard Sun, and Yoon Kah Leow (Best Paper Award Nominee)

3:30 – 4:00 pm: Afternoon Break

4:00 – 5:30 pm Session 6: Commemoration for Professor Te Chiang Hu

Session Chair: Andrew B. Kahng (UC San Diego)

"Influence of Professor T. C. Hu's Works on Fundamental Approaches in Layout," Andrew B. Kahng (UC San Diego, invited)

"Tree Structures and Algorithms for Physical Design," Chung-Kuan Cheng (UC San Diego, invited)

"Pioneer Research on Mathematical Models and Methods for Physical Design," Chris Chu (Iowa State University, invited)

"Theory and Algorithms of Physical Design," Te Chiang Hu, Chung-Kuan Cheng, and Andrew Kahng (UC San Diego, invited**)**

6:00 – 8:30 pm: Dinner Banquet

WEDNESDAY, March 28

8:30 am – 10:00 am Session 7: Interconnect Optimization and Detailed Routing Contest Results

Session Chair: Jackey Yan (Cadence Design Systems Corp.)

"Interconnect Optimization Considering Multiple Critical Paths," Jiang Hu, Ying Zhou, Yaoguang Wei, Steve Quay, Lakshmi Reddy, Gustavo Tellez, and Gi-Joon Nam

"Interconnect Physical Optimization," Charlie Janac, (Arteris Inc., invited)

"ISPD 2018 Initial Detailed Routing Contest and Benchmarks," Wen-Hao Liu (Cadence Design Systems Inc., invited)

10:00 – 10:30 am: Morning Break

10:30 am – 12:00 pm Session 8: How to Make Your Foundry Happier?

Session Chair: Jiang Hu (Texas A&M University)

"The Pressing Need for Electromigration-Aware Physical Design," Jens Lienig (Dresden University, invited)

"On Coloring and Colorability Analysis of Integrated Circuits with Triple and Quadruple Patterning Techniques," Alexey Lvov, Gustavo Tellez, and Gi-Joon Nam

"Standard CAD Tool-Based Method for Simulation of Laser-Induced Faults in Large-Scale Circuits," Raphael Viera, Philippe Maurine, Jean-Max Dutertre, and Rodrigo Possamai Bastos

12:00 pm – 12:10 pm: Closing Remarks

12:10 – 1:30 pm: Lunch

After Lunch: Social Activity