2013 International Symposium on Physical Design

With a Tribute to Professor Y. Kajitani

The Ridge Tahoe, Stateline, Nevada, March 24-27, 2013

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TENTATIVE ADVANCE PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI and biological systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance optimization and design for manufacturing.

Invited talks are 30 minutes. Regular presentations are 25 minutes. Short presentations (S) are 15 minutes. (EDS) presentations are 15 minutes, followed by a poster session. Best paper nominees are indicated by (bpn).

SUNDAY, March 24

5:30 – 7:00 pm: Evening Reception
(Location: Valley View Room)

MONDAY, March 25

8:30 – 9:45 am: Welcome and Keynote Address
(Location: Hungry Bear)

Host: Cheng-Kok Koh (*Purdue University*)

Keynote Talk: Heterogeneous 3-D Stacking, Can We Have the Best of Both (Technology) Worlds?
- Liam Madden (Xilinx)

9:45 – 10:15 am: Morning Break
(Location: Valley View Room)

10:15 am – 12:05 pm Session 1: 3D Integration and Physical Planning
(Location: Hungry Bear)

Chair: Markus Olbrich (University of Hannover)

(Invited) Physical-Aware System-Level Design for Tiled Hierarchical Chip Multiprocessors
- Jordi Cortadella, Javier de San Pedro, Nikita Nikitin and Jordi Petit (Universitat Politecnica de Catalunya, Barcelona)

Utilizing 2D and 3D Rectilinear Blocks for Efficient IP Reuse and Floorplanning of 3D-Integrated Systems
- Robert Fischbach, Johann Knechtel and Jens Lienig.

Benchmarking for Research in Power Delivery Networks of Three-Dimensional Integrated Circuits
- Pei-Wen Luo, Chun Zhang, Yung-Tai Chang, Liang-Chia Cheng, Hung-Hsie Lee, Bih-Lan Sheu, Yu-Shih Su, Ding-Ming Kwai and Yiyu Shi.

(Invited) High Performance and Low Power Design Techniques for ASIC and Custom in Nanometer Technologies
- David Chinnery (Mentor Graphics)

12:05 – 1:30 pm: Lunch
(Location: Tahoe A & B Room)

1:30 – 3:20 pm Session 2: Validation and Design for Yield
(Location: Hungry Bear)

Chair: Yao-Wen Chang (National Taiwan University)

(Invited) Electromigration and Its Impact on Physical Design in Future Technologies
- Jens Lienig (Dresden University of Technology)

(Invited) Data Mining in Design and Test Process – Basic Principles and Promises
- Li.-C. Wang (UC Santa Barbara)

SRAM Dynamic Stability Verification by Reachability Analysis with Consideration of

Threshold Voltage Variation
- Yang Song, Sai Manoj Pudukotai Dinakarrao, Hao Yu and Guoyong Shi

PushPull: Short Path Padding for Timing Error Resilient Circuits
- Yu-Ming Yang, Iris Hui-Ru Jiang and Sung-Ting Ho.

3:20 – 3:50 pm: Afternoon Break (Location: Valley View Room)

3:50 – 5:50 pm Session 3: Commemoration for Professor Y. Kajitani (Location: Hungry Bear)

Chair: Prof. Yasuhiro Takashima (University of Kitakyushu), Jiang Hu (Texas A&M University)

(Invited) Dawn of Computer-aided Design - from Graph-theory to Place and Route
- Atsushi Takahashi (Tokyo Institute of Technology)

(Invited) Practicality on Placement Given by Optimality of Packing
- Shigetoshi Nakatake (The University of Kitakyushu)

(Invited) On the Way to Practical Tools for Beyond Die Codesign and Integration
- Hung-Ming Chen (National Chiao-Tung University)

(Invited) Coding the Objects in Place and Route CAD
- Yoji Kajitani (Japan Advanced Institute of Science and Technology)

6:15 – 8:45 pm: Dinner Banquet – Honoring Professor Y. Kajitani (Location: Eagles Nest (off site))
Chair: Yasuhiro Takashima (University of Kitakyushu)

TUESDAY, March 26

8:30 – 10:20 am Session 4: Advanced Technologies and Design for Manufacturability (Location: Hungry Bear)

Chair: Ting-Chi Wang (National Tsing Hua University)

(Invited) Circuit and PD Challenges at the 14nm Technology Node
- James Warnock (IBM)

(Invited) Optical Lithography Extension with Double Patterning
- Shigeki Nojima (Toshiba)

A Structured Routing Architecture and its Design Methodology Suitable for High-throughput Electron Beam Direct Writing with Character Projection
- Rimon Ikeno, Takashi Maruyama, Tetsuya Iizuka, Satoshi Komatsu, Makoto Ikeda and Kunihiro Asada.

(bpn) Simultaneous OPC- and CMP-aware Routing Based on Accurate Closed-Form Modeling
- Shao-Yun Fang, Chung-Wei Lin, Guang-Wan Liao and Yao-Wen Chang.

10:20 – 10:45 am: Morning Break (Location: Valley View Room)

10:45 am – 12:30 pm Session 5: Routability and Routing (Location: Hungry Bear)

Chair: Jackey Yan (Cadence)

Planning for Local Net Congestion in Global Routing
- Hamid Shojaei, Azadeh Davoodi and Jeffrey Linderoth.

Escape Routing of Mixed-Pattern Signals Based on Staggered-Pin-Array PCBs
- Kan Wang, Huaxi Wang and Sheqin Dong.

Delay-Driven Layer Assignment in Global Routing under Multi-tier Interconnect Structure
- Jianchang Ao, Sheqin Dong, Song Chen and Satoshi Goto.

(S) SRP: Simultaneous Routing and Placement for Congestion Refinement
- Xu He, Wing-Kai Chow and Evangeline F.Y. Young.

(S) Case Study for Placement Solutions in ISPD11 and DAC12 Routablity-Driven Placement Contests
- Wen-Hao Liu, Cheng-Kok Koh and Yih-Lang Li.

12:30 – 2:00 pm: Lunch
(Location: Tahoe A & B Room)

2:00 – 3:50 pm Session 6: New Frontiers for Physical Design
(Location: Hungry Bear)

Chair: Ismail Bustany (Mentor Graphics)

(Invited) A Compiler for Scalable Placement and Routing of Brain-like Architectures
- Narayan Srinivasa (HRL Lab)

(Invited) Physical Design for Debug: Insurance Policy for IC's
- John Giacobbe (Intel)

A Top-Down Synthesis Methodology for Flow-Based Microfluidic Biochips Considering Valve-Switching Minimization
- Kai-Han Tseng, Sheng-Chi You, Jhe-Yu Liou and Tsung-Yi Ho.

(bpn) Designing VeSFET-based ICs with CMOS-oriented EDA Infrastructure
- Xiang Qiu, Malgorzata Marek-Sadowska and Wojciech Maly.

3:50 – 4:15 pm: Afternoon Break
(Location: Valley View Room)

4:15 – 5:45 pm Session 7: Expert Designer/User Session (EDS)
(Location: Hungry Bear)

Chair: Laleh Behjat (University of Calgary)

(EDS) Design and Tuning of a Tree-Mesh Clock Distribution
- Nikhil Jayakumar, Dave Murata and Valery Kugel (Juniper Networks)

(EDS) Automated Large Block Placement Strategies
- Gregory Ford (IBM)

(EDS) Structured APR: A Hybrid Approach for Efficient Custom Design
- Atul Walimbe, Robert Sweeney, Sumit Goswami and Raj Varada (Intel)

(EDS) Electrical Variability due to Layout Dependent Effects: Analysis, Quantification, and Mitigation on 40 and 28nm SOC Designs
- Mark Zwolinski, Yangang Wang (University of Southampton), Andrew Appleby, Mark Scoones, Sonia Caldwell, Touqeer Azam (Cambridge Silicon Radio Ltd), Philippe Hurat and Chris Pitchford (Cadence Design Systems)

(EDS) iDFM Flow: An ECO Implementation of Metal, Via Filling
- Giriraj Kakol, Dibyendu Goswami, Rajesh Karturi and Suryanarayana Prekke (Intel)

(EDS) Clock Enable Timing Closure Methodology
- Harish Dangat (Samsung)

5:45 – 6:15 pm EDS Posters and Discussion
(Location: Hungry Bear)

6:15 – 8:45 pm: Dinner Banquet
(Location: Tahoe A & B Room)

WEDNESDAY, March 27

8:30 – 10:30 am Session 8: Logic, Clock Driven PD and beyond
(Location: Hungry Bear)

Chair: Aiqun Cao (Synopsys)

(Invited) Relative Timing Driven Multi-Synchronous Design: Enabling Order-of-Magnitude Energy Reduction
- Ken Stevens (University of Utah)

(bpn) Network Flow Based Datapath Bit Slicing
- Hua Xiang, Minsik Cho, Haoxing Ren, Matthew Ziegler and Ruchir Puri.

(bpn) FF-Bond: Multi-bit Flip-flop Bonding at Placement
- Chang-Cheng Tsai, Yiyu Shi, Guojie Luo and Iris Hui-Ru Jiang.

Buffer Sizing for Clock Networks Using Robust Geometric Programming Considering Variations in Buffer Sizes
- Logan Rakai, Amin Farshidi, Laleh Behjat and David Westwick.

(S) Local Merges for Effective Redundancy in Clock Networks
- Rickard Ewetz and Cheng-Kok Koh.

10:30 – 11:00 am: Morning Break
(Location: Valley View Room)

11:00 am – 12:00 pm Session 9: TAU/ISPD Joint Session on Contests
(Location: Hungry Bear)

Chair: Charles Liu (TSMC)

An Improved Benchmark Suite for the ISPD 2013 Discrete Cell Sizing Contest
- Muhammet Mustafa Ozdal, Chirayu Amin, Andrey Ayupov, Steven Burns, Gustavo Wilke, Cheng Zhuo

TAU 2013 Variation Aware Timing Analysis Contest
- Debjit Sinha, Luis Guerra e Silva, Jia Wang, Shesha Ragunathan, Dileep Netrabile, Ahmed Shebaita

12:00 – 12:10 pm: ISPD Closing Remarks
(Location: Hungry Bear)

12:10 – 1:30 pm: TAU/ISPD Keynote and Lunch
(Location: Tahoe A & B Room)

Chair: Chirayu Amin (Intel Corporation)

Opportunities and Challenges for High Performance Microprocessor Designs and Design Automation
- Ruchir Puri (IBM)

1:30 – 2:00 pm: Afternoon Break and TAU Opening Remarks
(Location: Valley View Room)

2:00 – 3:30 pm: TAU/ISPD Invited Session: What Will It Take to Tame the Hierarchical Design Trolls?
(Location: Hungry Bear)

Chair: Tom Spyrou (Altera)

To Do or Not to Do Hierarchical Timing?
- Florentin Dartu and Qiuyang Wu (Synopsys)

Variability Aware Hierarchical Implementation of Big Chips
- Vidyamani Parkhe (Mentor Graphics)

Challenges in Managing Timing and Wiring Contracts during Hierarchical Floorplanning and Design Closure
- Shyam Ramji (IBM)