ACM International Symposium on Physical Design 2009
Clock Network Synthesis Contest
Call for Participation (Updated Jan 7, 2009)

This is an announcement for the first clock network synthesis contest! During the past four years, ISPD has been hosting placement and global routing contests with relevant industrial benchmarks. In ISPD 2009, we continue this great tradition and host a new clock network synthesis contest. Clock distribution network synthesis is one of the most fundamental CAD problems, and with the ever increasing performance demands of today's VLSI chips this problem is getting ever more difficult. In a typical industrial physical design flow, a separate dedicated clock network synthesis process is applied to build high performance minimum skew clock network, making it an excellent candidate as a new contest topic.

You are invited to participate!

Some important dates: The next ISPD will be held on March 29-April 1, 2009 in San Diego, California. The clock network synthesis contest will be held just prior to the symposium. To participate, contestants must register by January 21, 2009. The registration will allow you to receive a few sample benchmarks and relevant scripts to test your tool. The contest chair (Dr. Cliff Sze) will be running the tools from all teams on a single platform, so each contestant must submit their final clock network synthesis executable by March 2, 2009.

The quality of clock network solution will be measured by the range of clock arrival time of any arbitrary pair of clock sinks within a given slew constraint, simulated with different supply voltages to account for variation. In other words, all sinks must meet a given slew constraint and the clock network solution with the smallest range of clock latency value wins the contest. For simplicity, we will not consider CPU time, clock latency at this time. A clock network synthesis solution must be obstacle-aware, which means that it must be able to deal with blockages where clock buffers cannot be placed, but clock wires can route over blockages (since the clock typically uses a dedicated metal layer in any case). Clock latency measurement will base on spice-level circuit simulation. We are going to use an open source spice simulator in this contest. For more information, please visit our website at http://www.ispd.cc/contests/

As in previous contests, throughout the event, a new set of industrial clock network synthesis benchmarks will be released to further spur development in this area. The details of the contest designs will be posted to ISPD website later. We will also post the input and output file formats in details.

Please make note of the following:

- Cliff Sze from IBM Research will be chairing the contest. Any question about the contest should be directed to **csze@us.ibm.com**, with **subject "ISPD2009-CTS"**.
- All contest-related materials will be updated at: http://www.ispd.cc/contests
- To enter the contest, you must register by **January 21, 2009** by sending an email to the contest chair. Include the name of the tool, the names of the developers and the affiliation.
- On January 8, 2009, we will post a few sample benchmarks, the exact format of the input and output files, the buffer and wire library and their parasitic models for circuit simulation. Also, a script to translate your clock network synthesis output file into spice simulation input file will be provided.
- By February 23, 2009, each team must submit an "alpha-version" executable and a script to test it on our platforms. This is very important to make sure that our simulation results match yours.
- By March 2, 2009, a final-version executable, a script and a one-page description of your algorithm must be submitted to the contest chair.
- Results of the contest will be announced during ISPD 2009.