ISPD 2009 Clock Network Synthesis Contest

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IBM Research

Why this Contest Is So Different from the Previous?

- Placement and global routing
  - hard problems with “simple” rules
  - Wirelength, Overflow, etc…
- Clock network Synthesis
  - “Easy” sub-problems with complicated rules…
  - Why?

- Typical high performance clock network synthesis
  - More latency near the source
    - Hard to control skew
    - Trade power for robustness
  - Minimize power near clock sinks (e.g. latches, registers)

Overview

- Open contest primarily for academic community
- Totally 27 teams registered initially
  - Mostly academic teams and other from Intel, Cadence
  - 15.5 teams from US, 11.5 teams from overseas
    - 1 from Brazil
    - 2 from Canada
    - 1 from India
    - 5.5 from Taiwan
    - 2 from Hong Kong
- 16 alpha executables received by Feb 23
- 11 final entries by Mar 11 (1 team sent me just algorithm descriptions)
- 9 of them actually work
- Total 7 benchmarks
  - 1 derived from ISPD 2006 placement benchmark solutions
- Quality metrics
  - Minimize clock "skew" considering voltage variation
  - Constrained by total power

Teams around the world

JAN | FEB 23 | MAR 11

id	Name	Affiliation	Contact Author
1	team1	Georgia Institute of Technology	Xin Zhao
2	team2	University of Texas at Austin	Anurag Kumar
3	EKSS	NCKU CSIE, Taiwan	Chun-Hsien Lin
4	team4	National Taiwan University	Xin-Wei Shih
5	team5 ☆	UFRGS	Gustavo Wilke
6	team6 ☆	University of Michigan	Dongjin Lee
7	team7	University of California at Santa Cruz	Matthew Guthaus
8	team8	University of California at San Diego	Neelmani Kumar
10	team10	University of Texas at Dallas	Elizabeth Kiefer
11	Qian-Li-Ma	Purdue University and National Tsing Hua University	Yu-Ting Lee
12	UCSDCTS	Dept of Computer Science & Eng, University of California at San Diego	Renshen Wang
13	team13	IIT Bombay (Cadence)	Hari
14	team14	University of California at San Diego	Benjamin Cichy
15	team15	University of Texas at Austin	Ashutosh Chakraborty
16	Quartz	National Chiao Tung University, Hsinchu, Taiwan	Lee-Chung Hsu
17	NCTUgogogo	National Chiao Tung University, Hsinchu, Taiwan	Wen-Hao Liu
18	team18	Chinese University of Hong Kong	Xiao Linfu
19	team19	Dept of Electronic & Information Eng, Polytechnic University of Hong Kong	Jingwei Lu
20	team20	University of Texas at Austin	Yilin Zhang
21	team21	University of Calgary	Logan Rakai
22	CNS	Intel Corporation	Rupesh S. Shelar
23	team23	Iowa State University VLSI CAD LAB	Yanheng Zhang
24	NCKUF4	National Cheng Kung University	Sheng Chou
25	team25	University of Illinois, Urbana-Champaign	Ying-Yu Chen
26	team26	University of Michigan	Vincentius Robby
27	team27	University of Texas at Austin	Suhail Ahmed

☆ Thank the two teams who gave me preliminary binaries during late January/early February which facilitates my testing to the infra-structure.

Evolution of the contest

- Mid 2008, discussion on a new contest after placement and routing
  - 8 possible topics
  - Briefly agree on “Clock Tree Synthesis”
- November 2008, discussion with clocking experts in IBM
  - William Migatz (ASIC clocking)
  - Mehmet Yildiz (Clock routing)
  - Phillip Restle (uP clocking)
- Phillip contributed a lot on the contest format
  - Power limited
  - Real clock skew considering PVT variation
  - Non-tree is allowed
  - Uses SPICE timing
- December 24 – January 8
  - Finalize the contest rules, file formats
  - collect 45nm IBM technology information
  - Look for a public available SPICE simulation tool, SPICE model
  - A script such that SPICE simulation is (kind of) invisible to participants

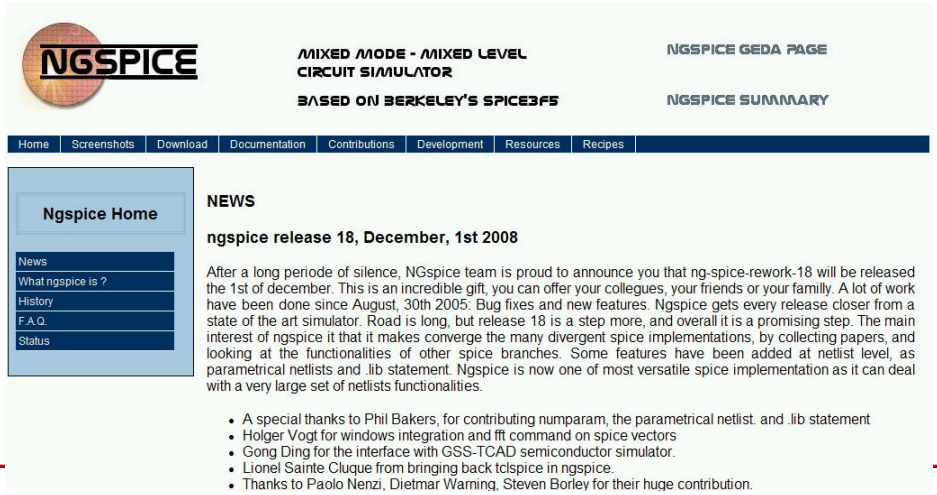
Contest formulations

- Realistic data for newer technology node
- Accurate delay calculation by SPICE
- Power limit
- Real clock skew considering variations

- Let’s experience the contest with me from the beginning… Watch out!! the road would be bumpy
- Are you ready?

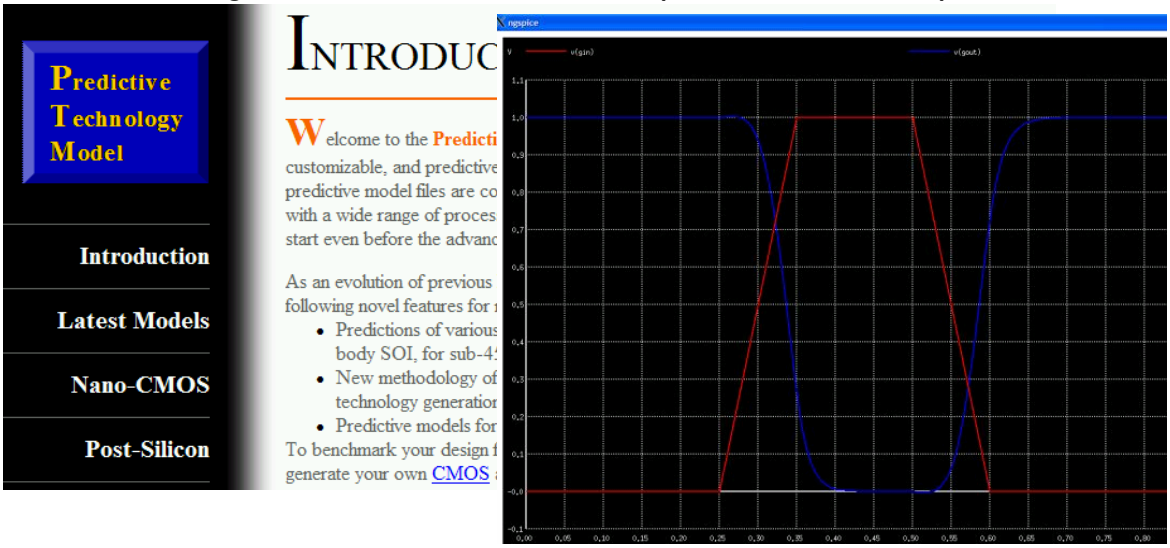
SPICE simulator

- Searching for public tools (instead of PowerSPICE)
- Thank Zhuo Li (IBM) for giving me his ngspice sample file
  - His sample file was for CADathlon 07
  - Used 180nm model from MOSIS ☹



Model cards

- Searching SPICE model for 45nm (instead of IBM's)



- Luckily, the HP model roughly matches what I have in IBM

Basic Contest Data

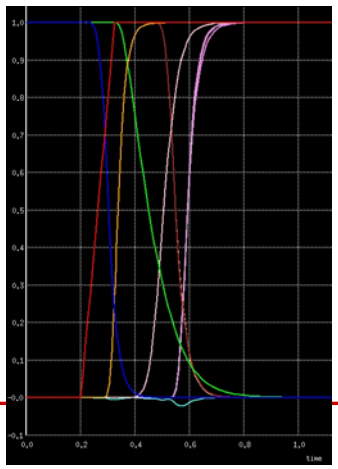
- Two inverters (45nm HP PTM model)
  - Mid-sized inverter
    - 10um nmos, 14.6um pmos (for similar R/F delay)
    - input cap = 35fF, resistance = 61.2Ohm, output parasitic cap = 80fF
  - small inverter
    - 1.37um nmos, 2um pmos
    - input cap = 4.2fF, resistance = 440Ohm, output parasitic cap = 6.1fF
- Two wire types
  - Loosely based on IBM 45nm technology data
  - Wide wire = 0.1 Ohm/um 0.2 fF/um
  - Narrow wire = 0.3 Ohm/um 0.16 fF/um

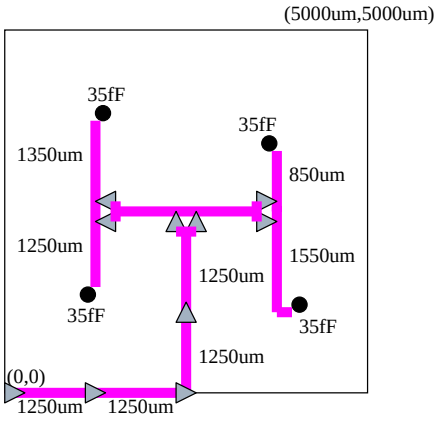
Basic Contest Data

- Mimic designs from uP to high-performance ASIC
- Clock frequency = 2GHz, Clock period = 500ps
- Slew (10%-90%) is limited within 100ps
- Clock source is at (0,0).
- The source is directly driving the mid-sized inverter.
- The input slew to this inverter is 100ps.
- Vdd = 1V

Try to simulate a sample clock tree

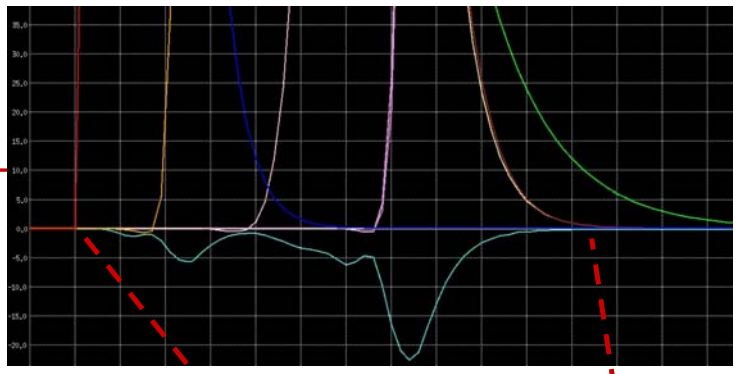
- 4 sinks, same load
- Located just off the centers of the 2x2 grid over 5mm x 5mm chip area
- Two inverters are connected in parallel at the center of the layout



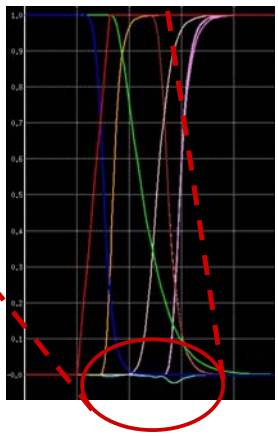


Inverters connected in parallel

Power Estimation



- We could use SPICE simulation and get the current of all voltage source
- However, it would be much simpler if we just use CV^2f
  - Total capacitance
    - Input load and output parasitic capacitance of all inverters
    - Wire capacitance
- Power limited
  - A tool is written to generate a simple clock tree with no slew violations
  - Power will be limited by (~1.5x to 2x ref. value)

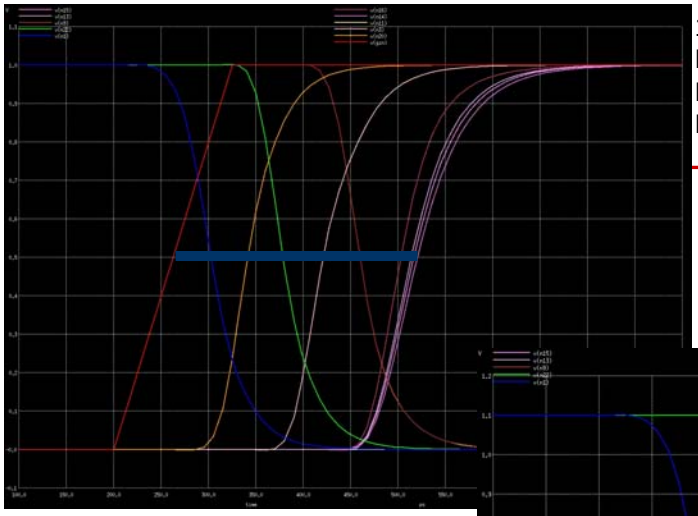


Robustness of Clock Network and Variations

- Monte Carlo simulations with different variables
- Too time consuming to run MC and SPICE for 26 teams x n benchmarks
- We need something simple
- Voltage variations?
- Two SPICE simulations (1V, 1.2V)
  - with all inverters being set to the same voltage each time

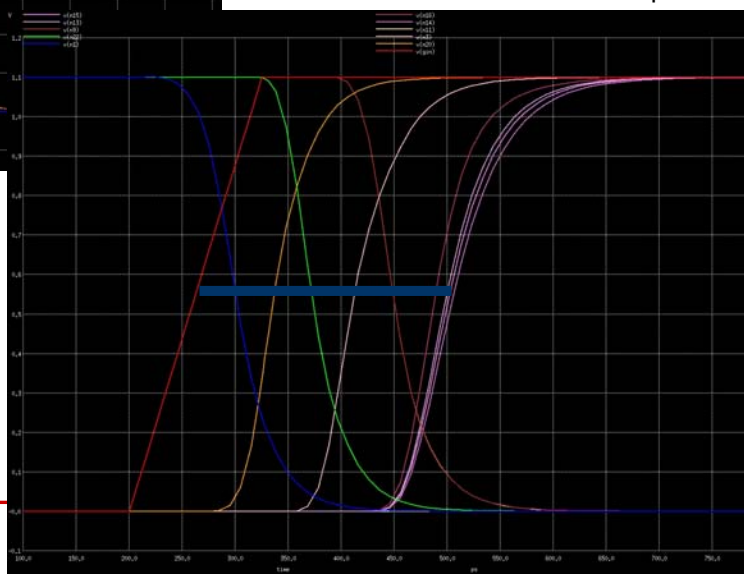
Clock Latency Range (CLR)

- On each voltage setting
  - SPICE simulation gives one set of clock latency values at all clock sinks
  - Nominal clock skew can be calculated
- For two voltage settings
  - Clock Latency Range : the maximum difference of clock arrival time of any arbitrary pair of clock sinks from the two supply voltage simulations.
- CLR is an upper bound of the actual skew
  - Actual skew = nominal skew “+” variations
- Winner has minimum CLR between 1V and 1.2V



1V
Min clock latency 240.5ps
Max clock latency 257.8ps
Nominal skew = 17.3ps

1.1V
Min clock latency 226.4ps
Max clock latency 243.4ps
Nominal skew = 17ps



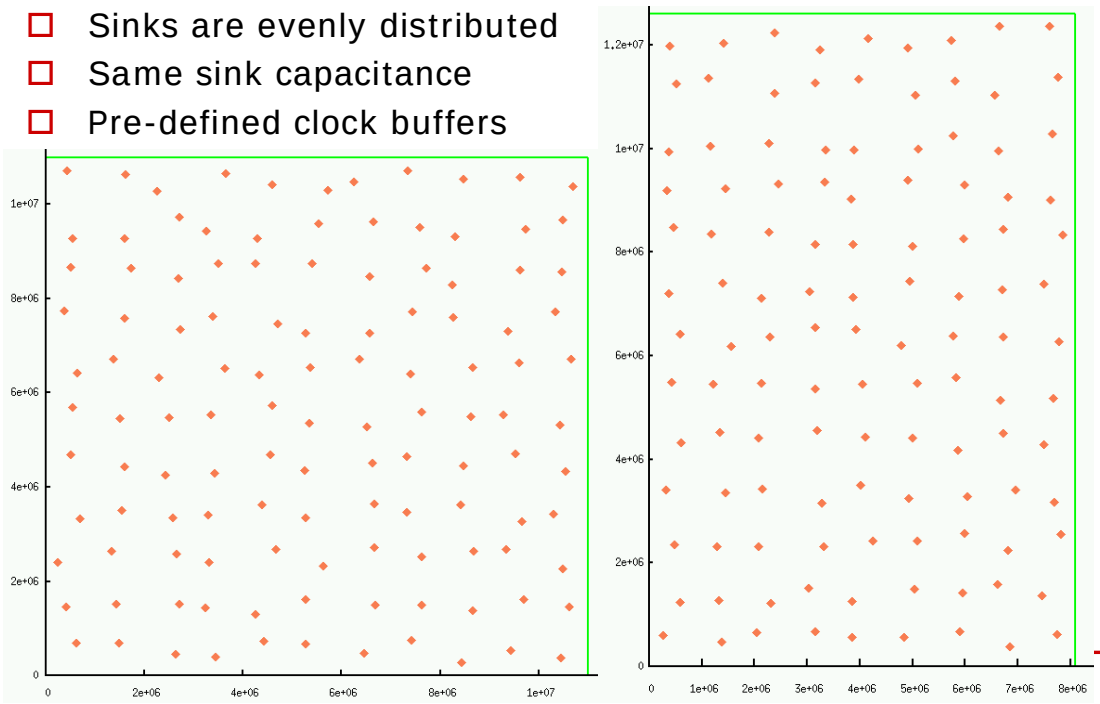
- "Actual skew" upper bound
  = clock latency range
  = 257.8 - 226.4
  = 31.4ps
- A script translates the clock tree into ngspice format
- Check slew at each inverter input and all clock sinks
- Calculate the clock latency at all clock sinks for 1V and 1.2V

Rules on Inverter Placement and Routing

- Inverter is modeled as a point
  - Representing both the input pin and output pin
  - Two buffers can be placed at the same coordinate
  - Buffer cannot be on top of a set of blockages
- Larger inverter can be formed by connecting two inverters in parallel
- Wire is modeled as two end-points
  - Two wires can have same end-points
  - Wire length is the Manhattan distance
  - No routing blockages
    - Reserved routing resources are usually available
  - Wire will be segmented to be less than 500um when translating into R,C in ngspice format (resistive shielding effect)

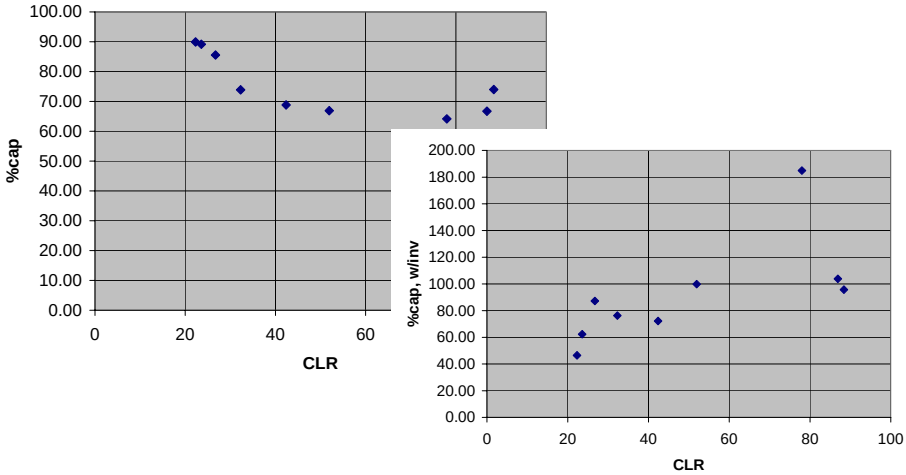
Benchmarks – Type 1 (ispd09f11, ispd09f12)

- Sinks are evenly distributed
- Same sink capacitance
- Pre-defined clock buffers



ispd09f11

- Cap limit
  - 118000

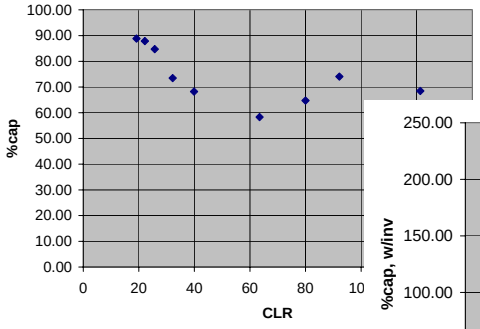


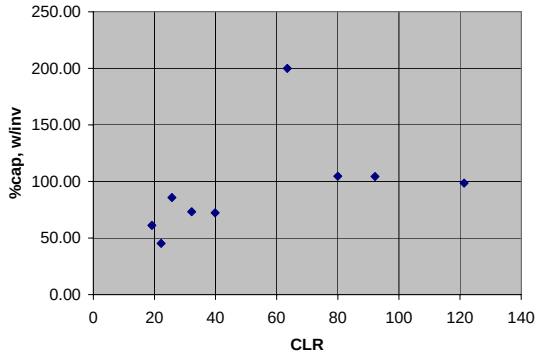
				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	26.71	100921.966	85.53	4235	51635	45051.966	87.25	14764	4.712	2
6	32.291	87156.965	73.86	4235	47035.8	35886.165	76.30	3892	5.166	3
7	86.901	78705.35	66.70	4235	36535.8	37934.55	103.83	733.88	44.576	6
11	51.94	78910.121	66.87	4235	37375	37300.121	99.80	0.2	9.504	4
17	22.306	106084.466	89.90	4235	69520.8	32328.666	46.50	23358	6.345	1
18	23.573	105213.969	89.16	4235	62215	38763.969	62.31	1113.67	10.452	8
19	42.387	81182.592	68.80	4235	44678	32269.592	72.23	587.39	8.673	8
21	88.388	87272.216	73.96	4235	42435	40602.216	95.68	1369.81	19.039	7
24	77.987	75672.665	64.13	4235	25070	46367.665	184.95	1.05	20.116	5

slew V
slew V

ispd09f12

- Cap limit
  - 110000



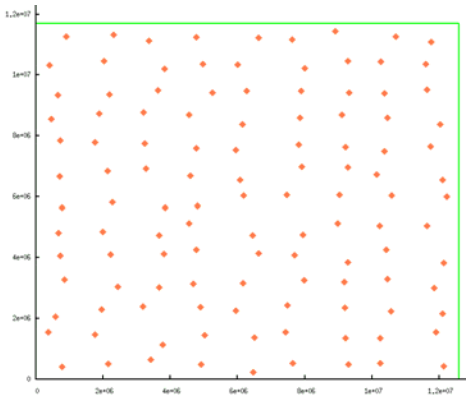


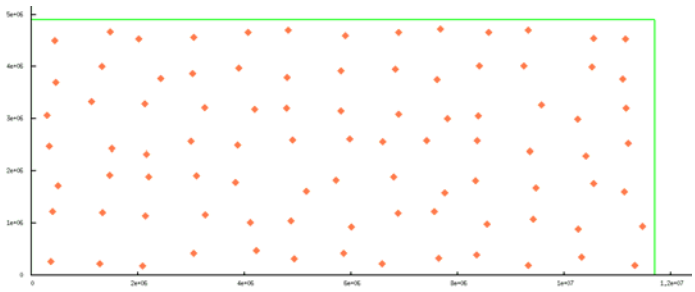
				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	25.728	93189.213	84.72	4095	47955	41139.213	85.79	13934	4.763	2
6	32.173	80796.821	73.45	4095	44275.8	32426.021	73.24	3944	5.883	3
7	121.328	75332.894	68.48	4095	35876.6	35361.294	98.56	830.64	87.857	8
11	80.015	71179.683	64.71	4095	32775	34309.683	104.68	0.16	39.673	6
17	22.175	96650.134	87.86	4095	63717.5	28837.634	45.26	14992	5.44	1
18	19.14	97720.95	88.84	4095	58075	35550.95	61.22	1104.79	9.644	9
19	39.851	75065.18	68.24	4095	41197	29773.18	72.27	484.87	8.824	4
21	92.173	81441.821	74.04	4095	37835	39511.821	104.43	1131.43	26.029	7
24	63.475	64132.14	58.30	4095	20010	40027.14	200.04	0.83	13.995	5

slew V

Benchmarks – Type 2 (ispd09f21, ispd09f22)

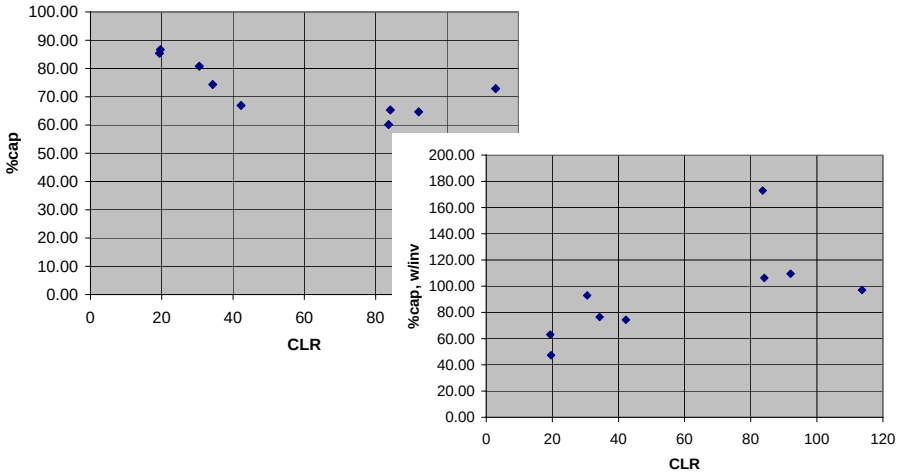
- Sinks are evenly distributed
- Different sink capacitance
- Clock buffers with different sizes tuned based on latch distributions





ispd09f21

- Cap limit
  - 125000

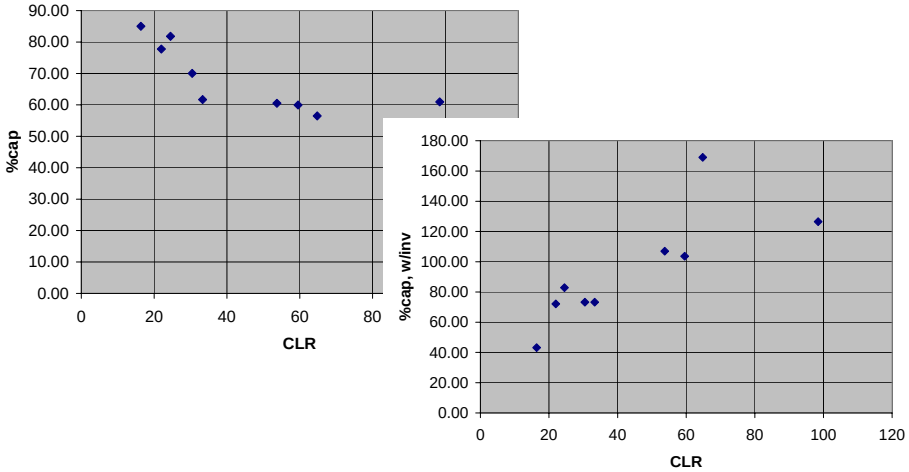


				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	30.536	100987.823	80.79	3587	50485	46915.823	92.93	14978	5.266	2
6	34.314	92880.351	74.30	3587	50602.6	38690.751	76.46	4587	6.077	3
7	92.053	80807.163	64.65	3587	36865.4	40354.763	109.47	846.5	48.111	7
11	84.128	81641.024	65.31	3587	37835	40219.024	106.30	0.18	38.833	6
17	19.61	108314.313	86.65	3587	71103.4	33623.913	47.29	26420	3.199	1
18	19.365	106723.687	85.38	3587	63250	39886.687	63.06	1056.29	7.183	9
19	42.26	83666.255	66.93	3587	45921	34158.255	74.38	696.24	8.347	4
21	113.669	91080.474	72.86	3587	44390	43103.474	97.10	1391.43	43.285	8
24	83.611	75160.217	60.13	3587	26220	45353.217	172.97	0.99	18.732	5

slew V

ispd09f22

- Cap limit
  - 80000

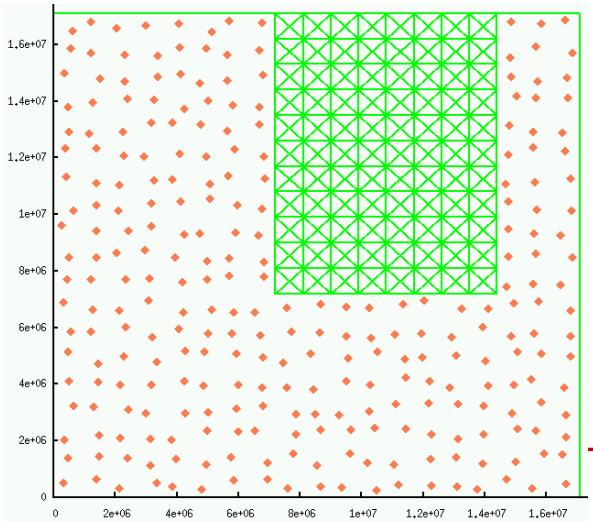


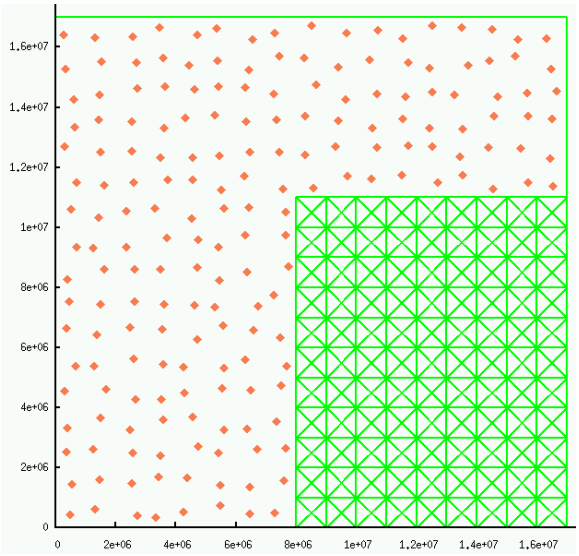
				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	24.505	65457.948	81.82	3427	33925	28105.948	82.85	7189	3.359	3
6	30.448	56006.581	70.01	3427	30355.4	22224.181	73.21	2005.37	7.099	4
7	59.541	47965.346	59.96	3427	21868.6	22669.746	103.66	406.15	26.189	6
11	53.733	48400.754	60.50	3427	21735	23238.754	106.92	0.12	21.597	5
17	16.376	68011.242	85.01	3427	45101.1	19483.142	43.20	9432	2.965	1
18	21.979	62218.067	77.77	3427	34155	24636.067	72.13	571.41	6	2
19	33.316	49341.435	61.68	3427	26499	19415.435	73.27	230.29	7.773	9
21	98.444	48751.091	60.94	3427	20010	25314.091	126.51	595.74	48.454	8
24	64.794	45193.32	56.49	3427	15525	26241.32	169.03	0.39	20.494	7

slew V

Benchmarks – Type 3 (ispd09f31, ispd09f32)

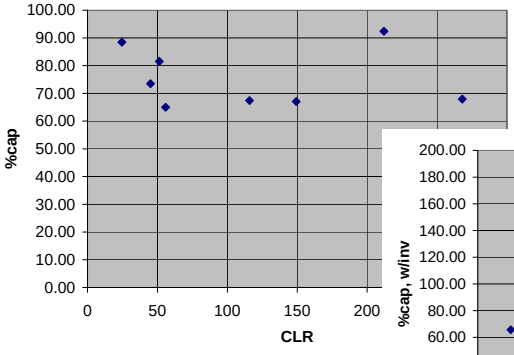
- Sinks are evenly distributed
- Different sink capacitance
- A big placement blockage
  - A different clock domain

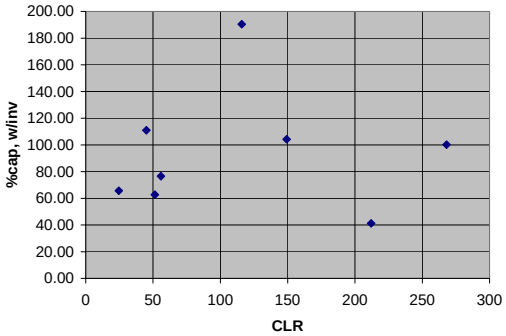




ispd09f31

- Cap limit
  - 250000





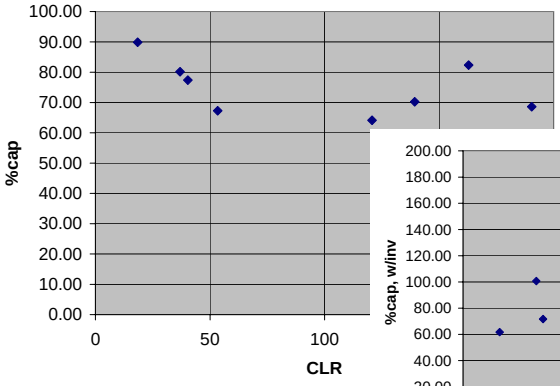
				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	45.068	183735.035	73.49	9555	82570	91610.035	110.95	40088	7.564	1
6	51.336	203827.343	81.53	9555	119370	74902.343	62.75	17333	10.867	2
7	268.069	169766.137	67.91	9555	80043	80168.137	100.16	2461.13	212.527	6
11	149.232	167634.557	67.05	9555	77395	80684.557	104.25	1.29	88.652	4
17	211.985	230938.038	92.38	9555	156778.8	64604.238	41.21	1.29	187.881	5
18	24.595	221196.737	88.48	9555	127765	83876.737	65.65	3565.58	10.191	7
19	55.821	162501.976	65.00	9555	86640	66306.976	76.53	2341.74	9.47	3
21	NA	NA	NA	NA	NA	NA	NA	NA	NA	7
24	115.884	168529.264	67.41	9555	54740	104234.264	190.42	8.13	21.143	7

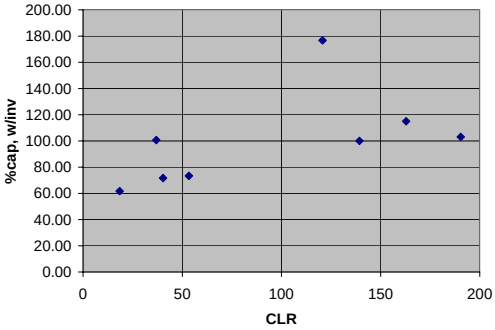
slew V

block V

ispd09f32

- Cap limit
  - 190000

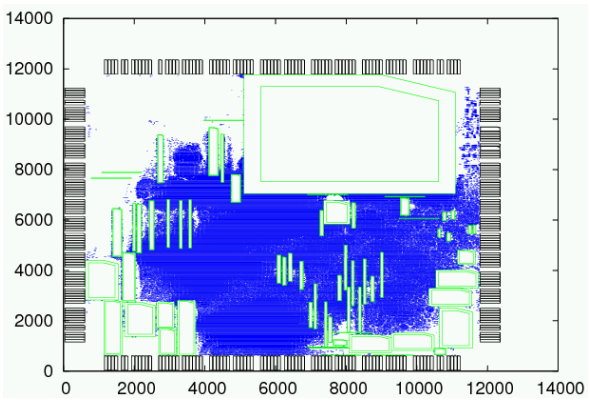


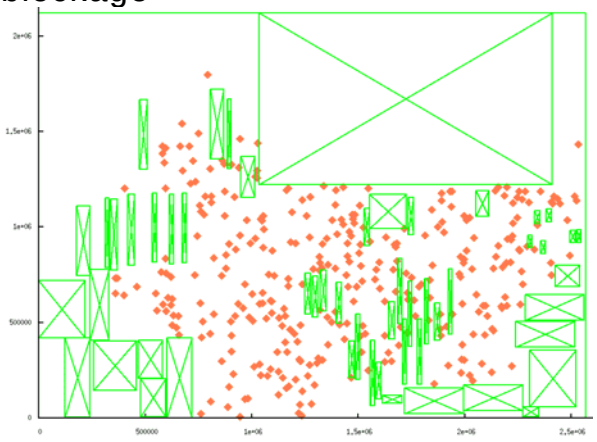


				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	36.901	152275.14	80.14	6650	72565	73060.14	100.68	3565.58	5.341	2
6	40.315	147037.936	77.39	6650	81776.6	58611.336	71.67	10599	6.44	3
7	190.416	130373.487	68.62	6650	60926.2	62797.287	103.07	1597.57	135.807	8
11	139.317	133421.194	70.22	6650	63365	63406.194	100.07	1.03	74.081	6
17	NA	NA	NA	NA	NA	NA	NA	NA	NA	9
18	18.418	170803.737	89.90	6650	101545	62608.737	61.66	2888.24	7.678	1
19	53.362	127771.814	67.25	6650	69881	51240.814	73.33	1384.23	8.501	4
21	162.879	156461.447	82.35	6650	69690	80121.447	114.97	3841	65.09	7
24	120.693	121866.339	64.14	6650	41630	73586.339	176.76	3.16	42.048	5

Type 4: Derive from real IBM ASIC design

- From the placement results of newblue1 (ispd09nb1)
- Randomly pick the latch locations
- Cluster latches and insert clock buffers as clock sinks of the contest benchmark
- No clock sink are inside any blockage





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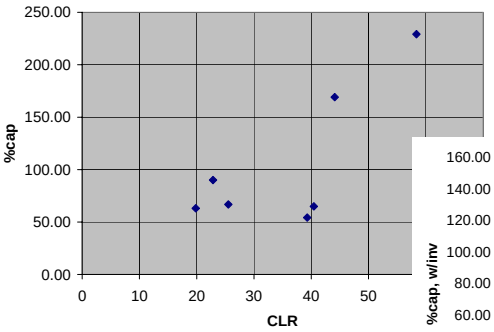
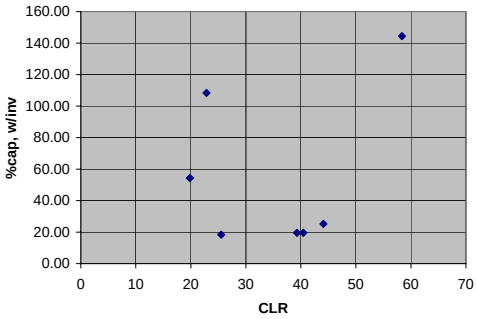
- Cap limit
  - 42000





				total cap					max	
id	CLR	CAP	%	sink	inverter	wire	w/inv(%)	CPU	nom skew	rank
4	NA	NA		NA	NA	NA	NA	NA	NA	5
6	19.835	26501.154	63.10	5919	13340	7242.154	54.29	477.37	7.228	1
7	40.455	27256.62	64.90	5919	13134.2	8203.42	19.53	895.33	25.977	5
11	39.291	22753.295	54.17	5919	8625	8209.295	19.55	0.31	23.733	4
17	NA	NA	NA	NA	NA	NA	NA	NA	NA	5
18	22.839	37793.715	89.99	5919	15295	16579.715	108.40	745.36	4.219	2
19	25.531	28055.333	66.80	5919	14406	7730.333	18.41	255.24	5.765	3
21	44.099	71017.083	169.09	5919	54510	10588.083	25.21	1506.65	23.634	5
24	58.367	96267.444	229.21	5919	29670	60678.444	144.47	0.71	30.272	5

block V

cap V

block & cap V

Final Results

- Top three stands out pretty clear from the others
- We are not going to distinguish 1st,2nd or 3rd because they are too close

			benchmarks							avg					
name	affiliation	id	11	12	21	22	31	32	nb1	rank	CLR	%cap	w/inv(%)	CPU(s)	nom skew
team4	National Taiwan University	4	2	2	2	3	1	2	5	2.43	31.57	81.08	87.82	13570.85	5.17
team6	University of Michigan	6	3	3	3	4	2	3	1	2.71	34.39	73.38	69.70	6119.68	6.97
team7	University of California at Santa Cruz	7	6	8	7	6	6	8	5	6.57	122.68	65.89	91.18	1110.17	83.01
Qian-Li-Ma	Purdue Univ & National Tsing Hua Univ	11	4	6	6	5	4	6	4	5.00	85.38	64.12	91.65	0.47	42.30
NCTUgogogo	National Chiao Tung University	17	1	1	1	1	5	9	5	3.29	58.49	88.36	44.69	14840.66	41.17
team18	Chinese University of Hong Kong	18	8	9	9	2	7	1	2	5.43	21.42	87.07	70.63	1577.91	7.91
team19	Polytechnic University of Hong Kong	19	8	4	4	9	3	4	3	5.00	41.79	66.39	65.77	854.29	8.19
team21	University of Calgary	21	7	7	8	8	7	7	5	7.00	99.94	88.87	93.98	1639.34	37.59
NCKUF4	National Cheng Kung University	24	5	5	5	7	7	5	5	5.57	83.54	85.69	176.95	2.18	23.83

- Winners are (in the order of team id)
  - Team4 – National Taiwan University
    - Xin-Wei Shih, Chung-Chun Cheng, Yuan-Kai Ho, Prof. Yao-Wen Chang
  - Team6 – University of Michigan
    - Dongjin Lee, Prof. Igor Markov
  - NCTUgogogo – National Chiao Tung University
    - Wen-Hao Liu, Hui-Chi Chen, Prof. Yih-Lang Li

Remarks on the Results

			benchmarks							avg					
name	affiliation	id	11	12	21	22	31	32	nb1	rank	CLR	%cap	w/inv(%)	CPU(s)	nom skew
team4	National Taiwan University	4	2	2	2	3	1	2	5	2.43	31.57	81.08	87.82	13570.85	5.17
team6	University of Michigan	6	3	3	3	4	2	3	1	2.71	34.39	73.38	69.70	6119.68	6.97
team7	University of California at Santa Cruz	7	6	8	7	6	6	8	5	6.57	122.68	65.89	91.18	1110.17	83.01
Qian-Li-Ma	Purdue Univ & National Tsing Hua Univ	11	4	6	6	5	4	6	4	5.00	85.38	64.12	91.65	0.47	42.30
NCTUgogogo	National Chiao Tung University	17	1	1	1	1	5	9	5	3.29	58.49	88.36	44.69	14840.66	41.17
team18	Chinese University of Hong Kong	18	8	9	9	2	7	1	2	5.43	21.42	87.07	70.63	1577.91	7.91
team19	Polytechnic University of Hong Kong	19	8	4	4	9	3	4	3	5.00	41.79	66.39	65.77	854.29	8.19
team21	University of Calgary	21	7	7	8	8	7	7	5	7.00	99.94	88.87	93.98	1639.34	37.59
NCKUF4	National Cheng Kung University	24	5	5	5	7	7	5	5	5.57	83.54	85.69	176.95	2.18	23.83

- Team18 - Chinese University of Hong Kong
  - Failed 3 benchmarks because slew is slightly (<1ps) over 100ps
  - Would have won the contest if they had set a guard band for slew
- Robust tools
  - I created another 10 difficult benchmarks while these two teams never fail any of them
    - Team6 - University of Michigan
    - Team24 - NCKUF4 - National Cheng Kung University

What did we learn?

- Most teams still focus on nominal clock skew
- Where is the non-tree structures (mesh, crosslinks)?
  - I intentionally change the contest name from “Clock Tree Synthesis (CTS)” to “Clock Network Synthesis (CNS)”
  - Maybe ~2x power budget is too low
  - I talked to the teams and found that non-tree is not widely used
    - Their experiments show little benefit
    - We need to dig deeper into this
- Inverter sizing to minimize gate delay
  - In turn, to minimize gate delay variations
  - Is it related to the observation of “smaller wire cap” leading to “smaller CLR”?
- This is just the first step
  - Feel free to study the results and I am sure there will be more findings
  - www.ispd.cc/contests